NANOTECHNOLOGY WORLD MAGAZINE

Nanotech Solutions for the Semiconductor Industry

Research

Liquid-metal synthesis of oxides opening up new applications for novel materials

Liquid metals were used as a successful reaction environment for the synthesis of desirable, atomically-thin layers of metal oxides that were unattainable using prior methods.

Interview

Paul Kirby is Senior Marketing Manager at Thermo Fisher Scientific

Why are FIB applications becoming pervasive in the fields of semiconductor metrology, analysis and characterization?

Testing

New solution rapid and high-quality testing

The number of transistors on a chip already reached 100 billion which is about 100 times more than the number of transistors on a chip produced in 2014. So, the need for fast quality control and non-destructive testing of wafers requires tools with much higher speed and accuracy in order to carry out the testing.

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FEATURES

Nanotechnology World Magazine
November 2022

Smarter, smaller, faster. Industry 4.0 requires innovation on a massive scale and nanotechnology has a lot to offer for the semiconductor industry.

Next issue:

Nanotech Solutions for the Energy Sector
February 2023

Nanotechnology is Set to Play an Important Role in Next-Gen Semiconductor Technologies

Found in everything from household appliances to cars and fighter jets, semiconductors play a vital role in the global economy. The semiconductor shortage isn't just affecting smartphones; the tiny chips are vital to our modern life and increasingly central to national security.

Over the past decades, the world has been growing its reliance on technology at an accelerating pace. Today's devices are getting increasingly smaller, energy and performance efficient, cheaper and smarter -- each generation of technology pushing these boundaries ever further. Silicon has transformed the electronics industry, but there comes a point at which conventional manufacturing methods and materials will no longer be able to meet the growing demands and expectations for progress without taking a quantum leap.

Semiconductors are at the core of modern-day technology and the ability to continue miniaturizing electronics hinges on utilizing effective semiconductor materials at the nanoscale, as modern-day technology is at the brink of a paradigm shift and is turning to the quantum world for solutions. While quantum technologies have the potential to create much faster and safer computing systems, the entanglement of qubits at the fundamental level will most likely rely on leveraging the quantum effects exhibited by nanoscale semiconductor materials.

On a global level, geopolitical issues, trade wars, material shortages and the pandemic have all played a part in disrupting the global supply chain creating semiconducting chip shortages. Switching to different manufacturing methods using nanomaterials could pave the way for new supply chain approaches that are not governed by the current constraints and challenges.

In the US, the CHIPS Act will impact where and how semiconducting devices will be created, and will help spur the development of a new infrastructure to help generate the large scales needed to provide for the growing societal and technological demand.

Investment in nanofabrication methods and the ability to create different nanomaterials with tailored semiconducting properties will help prevent future shortages, while enabling the development of smaller and better devices than current conventional manufacturing can provide, and give the industry a chance to keep up with the continuously increasing demand that awaits in the decades ahead.

Marine Le Bouar
Founder and CEO, Nanotechnology World Association
Editor in Chief, Nanotechnology World Magazine

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Dec 14-16, 2022
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IS&T Electronic Imaging 2023
IS&T International Symposium on Electronic Imaging
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Jan 15-19, 2023
Science Congress Center Munich, Germany

EMA 2023: Basic Science and Electronic Materials Meeting
Conference on Electronic and Advanced Materials
Jan 17-20, 2023
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SEMICON Korea 2023
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Coex, Seoul, South Korea

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Liquid-metal oxides opening routes to future technologies

Abigail Goff (RMIT) and Prof Michael Fuhrer (Monash)

Liquid-metal synthesis of oxides opening up new applications for novel materials

A liquid-metal discovery at RMIT University in Australia has been described as a 'once-in-a-decade' advance [1] .

Liquid metals were used as a successful reaction environment for the synthesis of desirable, atomically-thin layers of metal oxides that were unattainable using prior methods.

"It's a process so cheap and simple that it could be done on a kitchen stove by a non-scientist," said lead researcher Dr Torben Daeneke (RMIT) at the time.

Metals liquid at room temperature (or at relatively low temperatures) such as gallium (30°C), indium (157°C), bismuth (157°C), and tin (232°C) are ideal for the growth of new materials as their oxides may be printed and implemented into devices [2].

Alternatively, they can be alloyed with high-melting-point metals prior to oxidation, which expands the range of possible materials [3, 4] .

When a liquid metal is exposed to oxygen, a self-limiting chemical reaction (the Cabrera Mott process) forms a metal-oxide layer with a precise thickness of only a few atoms. The environment in which these two-dimensional (2D) surface 'skins' are grown can also be varied to allow for the synthesis of 2D materials other than oxides (e.g. exposure to hydrogen sulphide produces 2D metal sulphide layers), again expanding the range of possibilities.

For example, liquid-metal techniques are now being applied in:

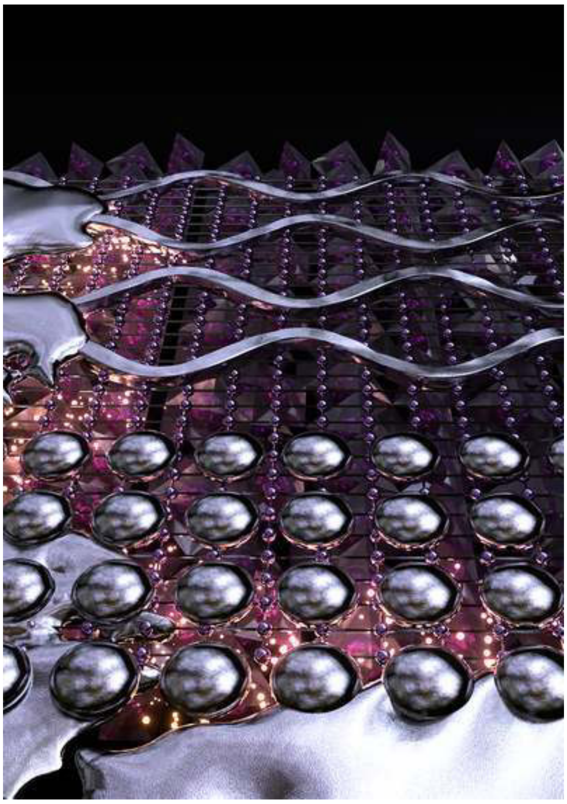
- liquid-metal touch printing of new electronic materials such as semiconductors or dielectric layers for beyond-CMOS transistors

- protective layers for delicate novel materials which enable integration into functioning devices

- never-before synthesized materials whose inherent properties may offer new applications

There are potential environmental advantages to the new technologies, addressing the embodied energy in silicon-based electronics. Synthesizing semiconductor-grade silicon, and processing it into devices, is very polluting, and consumes large amounts of energy. The new proposed methods are much less energy intensive, getting decent semiconductors from less-pure materials.

Liquid-metal touch materials printing in beyond-CMOS technologies



Two-dimensional materials have been shown to be superior replacements for silicon in 'beyond-CMOS' transistors. However many of these new 2D materials must be fabricated painstakingly by hand, by flaking tiny layers out of a bulk crystal of a layered material.

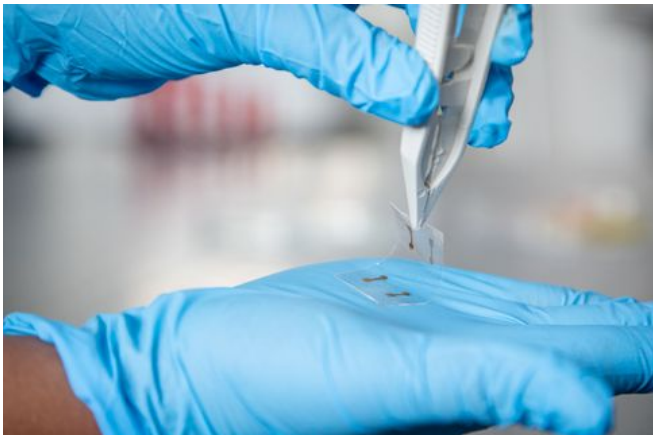
Liquid-metal touch printing offers an entirely new approach, and can produce 2D materials over large areas (as large as the size of the starting liquid-metal pool) with precisely controlled layer thickness at the atomic scale.

Moreover, liquid-metal touch printing is a 'gentle' process that can work at room temperature, making it particularly attractive for fabricating new types of flexible, transparent electronics on non-traditional substrates, which may not be amenable to high-temperature processes.

Liquid metals also provide high-quality materials. Liquids metals, with delocalised electron clouds, high surface tensions, and devoid of grain boundaries, sharp edges, or defects, are ideal reaction platforms for the growth of potentially defect and wrinkle free 2D materials.

New liquid-metal synthesized 2D materials are proving themselves in electronic devices. For example, liquid-metal printed 2D beta-tellurite, which fills a crucial need for a high-mobility p-type semiconductor layer to enable fast, transparent circuits [5] . This opens routes to wide-bandgap oxide-based electronics. These are robust (they are already oxidized, so they may not be affected by air), transparent (wide-bandgap materials), and could be used in applications such as transparent ('invisible') electronics, transparent TFTs for more energy efficient displays, or power electronics to charge batteries faster (car batteries, mobile phones etc).

Similarly, the unique electronic properties of 2D oxysulfides could be facilitated in next-gen electronic and optoelectronic devices [6] . The next step being pursued is the development of new types of chemistries, which can modify the deposited oxides and then tune the materials for tailored applications.



Protecting delicate materials

Liquid-metal printed materials have also been used to provide protection for other inherently-fragile novel materials, opening the way towards use of these materials in future technologies.

To unlock the significant potential of fragile 2D semiconductor materials in future electronic and optoelectronic devices, we must find a way to protect them in functional devices, while maintaining their key electronic and optical properties.

To date, the integration of 2D semiconductors into functional devices has been limited by their inherent fragility, or by the scalability of the protective materials being used.

Liquid-metal technology has addressed these issues by providing a high-performance, ultrathin, protective glass coating [7]. The new method of protection is cost-efficient and scalable, while maintaining the material's necessary electronic and optical properties. A reliable protection was demonstrated using ultrathin gallium-oxide (Ga_2O_3) glass as a scalable capping material for monolayer tungsten-disulfide (WS_2), which is a key 2D semiconductor.

Utilising new materials’ inherent properties

Other application of liquid metal materials harness the inherent properties of the new materials they allow synthesis of, including piezoelectricity, thermoelectricity or transparency [5].

For example, liquid-metal techniques [8] allow synthesis of atomically-thin tin-monosulfide (SnS), which has strong piezoelectric properties. The conversion of mechanical forces or movement into electrical energy in future device based on such materials could advance future flexible, wearable electronics, and biosensors drawing their power from the body’s movements.

The unprecedented technique of synthesis used involves van-der-Waals exfoliation of a tin sulphide formed on the surface of tin when it is melted, while being exposed to the ambient of hydrogen sulphide (H 2 S) gas. H 2 S breaks down on the interface and sulphurises the surface of the melt to form SnS.

The technique is equally applicable to other monolayer group IV monochalcogenide, which are predicted to exhibit the same strong piezoelectricity, for example atomically-thin indium-tin oxide [9] .

This property, along with their inherent flexibility, makes these materials likely candidates for developing flexible nanogenerators that could be used in wearable electronics or internal, self-powered biosensors.

Other applications and future directions

These are just three applications currently in use from the initial 2018 discovery. However there are many other applications being investigated, including using 2D synthesis in new, cooler catalyst applications to lower energy costs 10 , which can also be applied to carbon-capture technologies [11] .

The initial proof-of-concept electronic devices using liquid-metal technology are exciting, but there is still much more work to be done to understand how they can be manufactured reproducibly at scale.

FLEET researchers are also working to expand the range of elements which can be incorporated into liquid metal-synthesized 2D layers, and create materials with other desirable properties such as thermoelectrics or topological insulators.

But the capability to mass-produce atomically thin layers over large areas with a simple room-temperature process wasn't even dreamt of only a few years ago, and it is likely that the number of applications for the liquid-metal technique will continue to grow.

References on page 50

FLEET is the Australian Research Council Centre of Excellence in Future Low-Energy Electronics Technologies. FLEET.org.au

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Semiconductor Nanotechnology Alliance (SNA) promotes research and innovation in Hong Kong

The Alliance includes universities, industry leaders, investors, as well as local companies and associations.

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Interview

Jelena Trbovic is a nanotechnology expert and an applications manager at Zurich Instruments, where she manages lock-in amplifier business and develops business for quantum technologies. She received her PhD from Florida State University for research on semiconductor spintronics. As a postdoc at the University of Basel, she studied coherent transport in carbon nanotube quantum dots, graphene, and superconducting wires.

Transistors and integrated circuits are at the heart of the semiconducting industry. Ever since the transistor discovery in 1947 at Bell Labs [1], the group IV elements Silicon and Germanium have been at the center of the semiconducting chip industry allowing circuits density and their functionality to grow. As the fabrication and materials quality improved the chip density increased with the rate of density doubling approximately every 2 years [2]. In the last decade we have seen that the industry transitioned into the domain of nanotechnology simply because the circuit elements reached nanometer size. We now see IBM's Fin FET transistors with 2nm channel size [3] that cannot be reduced much further simply because the basic gate operations of the transistor will be unreliable and at some point, no longer possible due to the tunneling effects. Therefore, the solution will be in architecture innovation as well as reaching out to new materials and new technologies like nano – and quantum technologies.

How do you see semiconductors industry coping with current challenges?

Semiconductor industry is facing a number of challenges today, from reduced chips material supply, high energy consumption demands and increased need for new functionality and having to do more with less. Increased chip demand needs to be backed up with high production and testing capacity. Identifying and troubleshooting semiconductor device failures is also getting more challenging yet remains critical in order to reduce manufacturing costs and increase production capacity while maintaining quality.

The number of transistors on a chip already reached 100 billion [4] which is about two orders of magnitude more than the number of transistors on similar chips produced in 2014 [5]. So, the need for fast quality control and non-destructive testing of wafers requires tools with much higher speed and accuracy in order to carry out the testing.

What do you see as a solution to the rapid and high-quality testing?

I see it as a combination of new tools and new methods for wafer probing and testing.

Traditional laser voltage probing (LVP) and LVI (laser voltage imaging) are laser stimulation techniques used to test a device [6]. These methods have been widely used in the scanning mode while utilizing various frequency-dependent failure modes. Defect localization continues to be a challenge in the failure analysis field where the frequency dependent failure analysis is the key. This is where devices like modern lock-in amplifiers [7] available with a wide frequencies range and short time constants allow for a massive speedup with dwell times as short as 100 nanoseconds. They provide massive parallelism in time and frequency domain enabled by the on-board field programmable gate array (FPGA) boards with multiple oscillators and tools like Boxcar averager working seamlessly together in full capacity. For reliable testing the goal is to achieve a high signal-to-noise ratio (SNR) for both amplitude and phase of the measured signals. Thus, if we increase the SNR by a factor of 10 with better testing instrumentation that use lock-in amplifiers for example and use their parallel and multifrequency measurement capabilities (on the order of 10), we win a factor of 100 in the number of transistors on a modern chip.

How long can this trend continue, and do you see any other breakthroughs in the industry?

The approach of reducing the size of components and increasing the speed of the clock is not sustainable as it is very resource intensive and moreover it will not be able to deliver the performance demands of the next decade. The current power-hungry silicon-based chip technology could be replaced with nano-devices such as novel 2D materials: graphene, hexagonal boron nitride (hBN), molybdenum disulphide (MoS2), phosphorene (2D black phosphorus), or 1D semiconducting nanowires and carbon nanotubes.

The harbinger of the new nanomaterials trend is graphene, a one atom thick layer of graphite. It was first isolated by exfoliation from natural graphite in 2004 at the University of Manchester by Kostya Novoselov and Andre Gaim [8]. They demonstrated that this light material is stable in ambient conditions, and that it has superb charge transport properties, with charge carrier tunability and ultra-high mobilities which makes it a suitable candidate for novel transistor device structures. The bi-layer graphene showed a band gap that was also found in other 2D materials like hBN. What is even more surprising is the discovery of superconductivity by twisting the angle between the two sheets of a bi-layer graphene, magnetism and other cooperative phenomena deeming the future of the 2D materials and graphene even brighter. The large-scale sheets of graphene can be now produced using the chemical vapor deposition (CVD) method with carrier mobilities compared to the purest of exfoliated graphene [9]. Now it becomes clearer that with such versatile physical properties, we can design circuits with various functional characteristics on large-scale sheets of these novel 2D materials.

How do you see the current technology transitioning to nanotechnology and quantum computing with current resource and geopolitical challenges?

The current technology is not able to address all the needs of ever-growing amounts of data that require massive structuring and analysis, solving problems like large number factoring, finding solutions to complex optimization, physics and chemistry simulations and many more that today's computers cannot solve in practical time. We are seeing rapid advances in quantum computing with roots in nanotechnology. Quantum computers use qubits with massive parallel computing capability as opposed to classical bits with only two states available for computation. Today's dominant solid-state technology is based on micron sized superconducting circuit elements and nanosized Josephson junctions that are fabricated on quantum chips with over 100 qubits [10]. Solid hints of advantage of the technology compared to classical computation has been demonstrated by Google in 2019 [11].

There are still many challenges ahead that range from qubit material quality, control electronics required to readout the qubit state and run quantum algorithms with high efficiency. To tackle useful technological and business problems, quantum chips will need about 1 million qubits [12]. Several tech giants are set out to make such large number of superconducting quantum bits, however quantum chips with semiconducting spin qubits have even higher scalability potential due to their nanometer size [13]. They are based on quantum dots: zero dimensional nanostructures in silicon, germanium, Phosphorus doped silicon (Si-P), but also semiconducting nanowires, carbon nanotubes, graphene and 2D other materials.

Even though current geopolitical challenges bring tension and uncertainty there are many opportunities that will bring faster development of nano and quantum technologies when more funding and coordinated effort is distributed locally. We now see examples worldwide combining nanotechnology and quantum initiatives that will ensure a robust and scalable nano materials and quantum devices development geared up for the next generation of semiconducting industry processing units.

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hello tomorrow

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Mix and match' lithography paves the way for new semiconductor materials
University of Chicago (United States)

EV Group advances leadership in optical lithography

EV Group (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has announced that it has strengthened its portfolio of optical lithography solutions with the unveiling of the next-generation 200-mm version of its EVG®150 automated resist processing system. The redesigned EVG150 platform includes advanced features and enhancements that provide even greater throughput (by up to 80 percent) and versatility, as well as smaller tool footprint (by nearly 50 percent), compared to the previous-generation platform. The EVG150 provides reliable and high-quality coating and developing processes in a universal platform that supports a variety of devices and applications, including advanced packaging, MEMS, radio frequency (RF), 3D sensing, power electronics, and photonics. Its high throughput, flexibility and repeatability support the most demanding needs for both high-volume production and industrial development.

The EVG®150 automated resist processing system provides reliable and high-quality coating and developing processes in a universal platform that supports a variety of devices and applications, including advanced packaging, MEMS, radio frequency (RF), 3D sensing, power electronics, and photonics. Source: EV Group.

Silicon Austria Labs, a leading research center for Electronic Based Systems (EBS), is the first customer to receive the next-generation EVG150 system. “Through our cooperative research with leading manufacturers, we develop key technologies that build the foundation for Industry 4.0, IoT, autonomous driving, cyber-physical systems (CPS), AI, smart cities, smart energy, and smart health long before they reach the market,” stated Dr. Mohssen Moridi, Head of Research Division Microsystems of Silicon Austria Labs. “The high flexibility of EVG’s next-generation EVG150 resist processing system helps pave the way for high-volume implementation of new processes and products with our development customers that fuel EBS innovation.”

Universal platform provides unprecedented flexibility

The next-generation EVG150 for 200-mm substrates maintains the industry-leading capabilities of the previous-generation platform, including: fully automated platform with customizable module configurations for spin and spray coating, developing, bake and chill; EVG’s proprietary OmniSpray® technology for conformal coating of extreme topographies; sophisticated and field-proven robot handling with dual end effector capability to ensure continuous high throughput; and wafer-edge, bowed, warped and thin-wafer handling.

New features on the next-generation EVG150 200-mm platform include:

• Up to four wet processing module spaces and up to 20 bake/chill units, enabling the processing of many more wafers simultaneously

• Singulated coat chambers, providing complete isolation of modules and virtual elimination of cross-contamination between modules

• Further redesign of modules to enable easy access to individual chambers from outside of the tool, minimizing downtime and allowing for continued tool operation when conducting chamber maintenance

• Repositioning of chambers within the platform to enable easy access to robotic handling unit to facilitate maintenance

• Image-based pre-aligner to enable on-the-fly wafer centering for faster processing

• Integration of resist and chemistry lines inside the system, reducing external cabinet space for chemistry storage and reducing tool footprint

• Integration of user interface inside the system, further reducing tool footprint

The next-generation EVG®150 automated resist processing system maintains the industry-leading capabilities of the previous-generation platform while adding advanced features and enhancements that provide even greater throughput (by up to 80 percent) and versatility, as well as smaller tool footprint (by nearly 50 percent). Source: EV Group.

"Resist processing and patterning are the most repeated process steps in semiconductor manufacturing. EVG has built up many years of experience with these processes, including optical lithography and spin and spray coating, to address the needs of the most demanding customer requirements," stated Dr. Thomas Glinsner, corporate technology director at EV Group. "We've incorporated these learnings into our next-generation EVG150 system, which has been redesigned from the ground up to provide breakthrough throughput and cost-of-ownership benefits in a universal platform that offers unsurpassed flexibility to meet the widest variety of resist processing needs."

Product Availability

EVG is now accepting orders for the next-generation EVG150 automated resist processing system, and is offering product demonstrations at EVG's headquarters. For more information, please visit https://www.evgroup.com/products/lithography/resist-processing-systems/evg150/.

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Atomic Force Microscopy for Semiconductor Applications

Semiconductors are an essential component in many electronic devices employed in critical industries including computing, healthcare, transportation and many others. With such a wide reach, the semiconductor industry is continuously growing and innovating with the goal of producing more energy efficient, more reliable, and more affordable devices. In order to accomplish these goals, considerable effort is directed toward the R&D and QA/QC phases of the semiconductor production cycle. Atomic Force Microscopy (AFM) is an important tool for semiconductor characterization in that cycle. Specifically, surface roughness measurements, defect review and failure analysis are all areas where AFM excels and provides valuable information for semiconductor production process optimization.

Basic principles of AFM

AFMs are instruments used to visualize the topography of samples, as well as their mechanical, electrical and other properties. Unlike optical microscopes where light interacts with the sample to produce an image, AFM uses a sharp probe to "feel" the surface in the same way we can feel the surface under our finger. The probe used to characterize the surface is a sharp tip mounted on a cantilever. The tips are often microfabricated from silicon and the tip radii range from five to hundreds of nanometers (Figure 1A). The cantilever on which the tip is mounted on serves the role of the sensor of tip-sample forces.

To produce an image, the tip is raster scanned over the sample line by line. As the tip scans the surface, any changes in the surface topography are detected using the optical beam detection (OBD) setup. OBD is a laser beam focused on the back of the cantilever and then reflected into a photodetector (Figure 1B). As the tip interacts with the sample during the scan, the cantilever bends or deflects. This variation in cantilever deflection is recorded as change in position on the photodetector.

Raster scanning of the samples is achieved using piezoelectric actuators and flexures. Additionally, sensors in the x, y, and z directions assure quantitative measurements. In general, AFM images can vary in size from tens of nanometers to hundred microns. Vertical resolution of the features imaged depends on the AFM instrument noise, but a high performance AFM can even resolve atomic defects. Lateral resolution of AFMs is dependent on the tip radius, but is typically below 10 nm. AFM characterization is non-destructive, can be performed in ambient conditions and sample preparation is minimal.

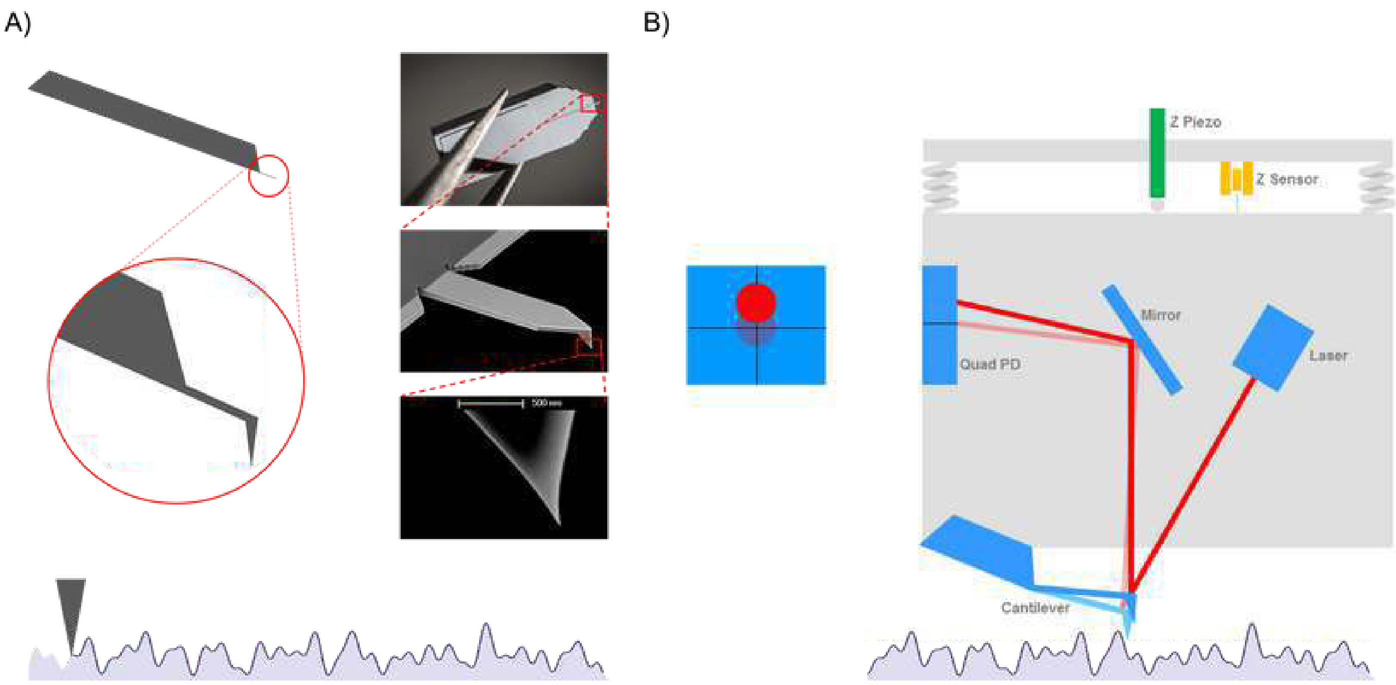

Fig. 1. *A) AFM probe schematic as well as optical and SEM images. B) Schematic of OBD detection setup used in AFMs.*

How is AFM used for semiconductor applications

Measurements of surface roughness and morphology are essential, whether to validate an individual processing step or to obtain a quality control metric for the final product. The choice of instrument best suited for surface roughness measurements depends strongly on the specific material being measured as well as on the expected size and shape of its surface features. As device dimensions in many industries continue to shrink, it is becoming increasingly important to characterize surface roughness at the scale of nanometers and even lower. Tools commonly used for this purpose include interferometric optical profilometers, scanning electron microscopes, and atomic force microscopes (See Figure 2). AFM is the only technique offering unparalleled three-dimensional spatial resolution, measure material characteristics such as electrical, mechanical and functional with the ability to measure most types of materials. AFM provides complete 3D surface quantification by imaging topography. Jupiter XR AFM was specifically designed for semiconductor related applications; it has the best noise and resolution performance, offers simplified user experience, and enables various imaging modes.

Ducey awards $100M for semiconductor boost

"Arizona has earned a place as one of the world's leading destinations for chip design, manufacturing and innovation," said Governor Ducey. "With historic opportunities before us, this funding ensures we make the most of this moment and cement our semiconductor leadership for decades to come. [Read more]

	Oxford Instruments Jupiter XR AFM	Scanning Electron Microscopes	Interferometric Optical Profilometers	Stylus Profilometers	Relevance
Lateral resolution	<1-20 nm	<1-20 nm	200-500 nm	1000-10,000 nm	Accurate nanoscale surface roughness measurements require nanometer-scale resolution.
Height resolution	<0.025 nm	No true 3D measurements possible	1-10 nm	0.5 nm	
Measurement type	Surface topography (3D) and surface properties*	Surface morphology (quasi-3D) and composition*	Surface topography	Line profiles (inefficient for surface mapping)	Areal surface roughness measurements require accurate imaging of 3D topography.
Measurement time (per site)	<1 minute	<10 seconds	<10 seconds	<1 minute	Throughput of multisite measurements is affected by time spent per site.
Surface material limitations	Any material type can be measured up 200 mm in diameter and 35 mm in height	Must be conductive (or coated) and vacuum compatible	Large variations in reflectivity and refractive index, steep slopes or edges, and very thin films can be problematic.	Most materials can be measured unless very soft and/or sticky	Many inspection tools have constraints on the types of materials that can be measured.

Fig. 2. *Comparison of tools for surface characterization. Specifications given for non-AFM tools are typical ranges for commercial instruments. Both AFMs and scanning electron microscopes can provide information about material properties beyond topography. For example, AFMs can measure a host of electrical (e.g. conductivity, permittivity), mechanical (e.g. elastic modulus), and functional properties (e.g. piezoelectric response).*

Roughness measurements are one of the most common AFM measurements since the AFM can deliver quantitative roughness data even at very low roughness values (S_a below 100 pm or 1 Å) thanks to the low noise floor of the instrument. Figure 3 shows two examples of AFM roughness measurements. The first set of images (Figure 3 A) is related to quality assurance of Atomic Layer Deposition (ALD) process. ALD was used to deposit Al_2O_3 film in a controlled manner so that the film thickness could be closely monitored. At the same time, it was important to keep the surface roughness low to maintain best performance of the film. AFM data provided roughness values increased from S_a = 2.1 Å at 50 nm thickness to S_a = 4.4 Å at 300 nm and started to level off to S_a= 5.6 Å at 800 nm and beyond. The second example (Figure 3B) is a roughness measurement of epitaxial silicon layer on a 150 mm wafer. Epitaxial layers are commonplace in modern semiconductor processing since silicon epitaxy processes allow precise layers with different dopant types and concentrations, while heteroepitaxial layers of III-V compounds and other materials enable even more options. An additional benefit of epitaxial layers is their extremely low surface roughness compared to substrates prepared by chemical-mechanical polishing. The AFM data here provides important information about the uniformity of the epitaxial layer depending on the position on the wafer; at the very edge of the wafer the roughness is Sa = 0.79 Å and closer to the center of the same wafer the roughness was measured to be Sa = 0.90 Å. The AFM images also show the change in the surface morphology depending on the position on the wafer. Semiconductor fabrication requires extreme level of cleanliness, as any contamination may result in device failure. For this reason, great care is taken to identify contamination and defects, and eliminate their sources. For example, when photomask blanks used for extreme ultraviolet lithography (EUV) processes are produced, the goal is to reduce the number of particles larger than ~20 nm, on a 6-inch photomask blank, to zero. Initial contamination inspection is done using light scattering to locate defects, but it cannot provide accurate information about defect type (i.e. particle vs. indent).

This is where AFM has become an indispensable tool used to easily identify very small contaminates and indicate if the contaminate is a particle, a hole defect, or a bump, while providing the exact defect location.

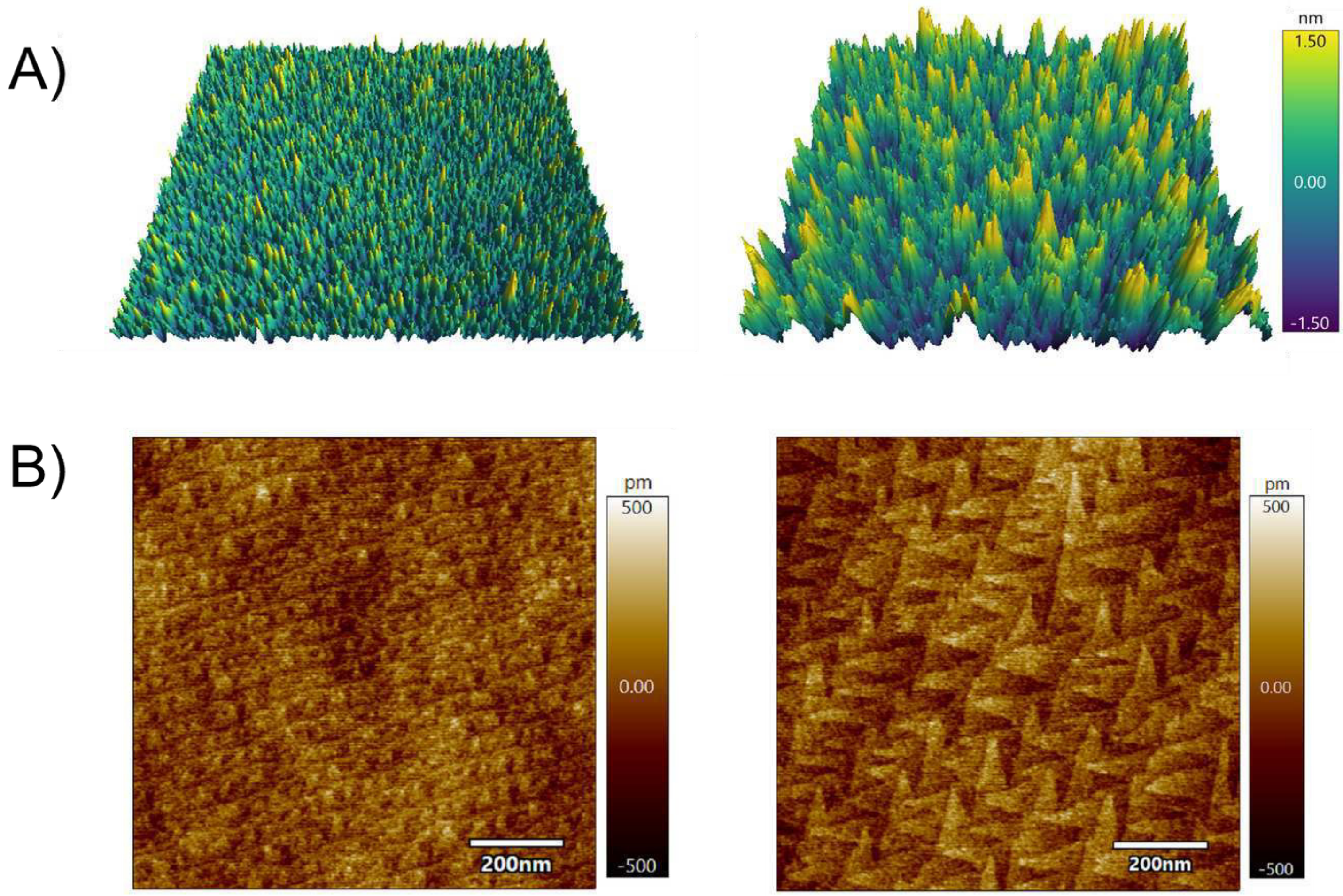

Fig. 3. *Examples of AFM roughness measurements. A) Increase of surface roughness of Al_2O_3 from S_a = 2.1 Å to S_a = 5.6 Å at 800 nm as the layer thickness increased from 50 to 800 nm. B) Roughness of epitaxial silicon wafer measured at the very edge of the wafer (S_a = 0.79 Å) and closer to the center of the same wafer (S_a = 0.90 Å)*

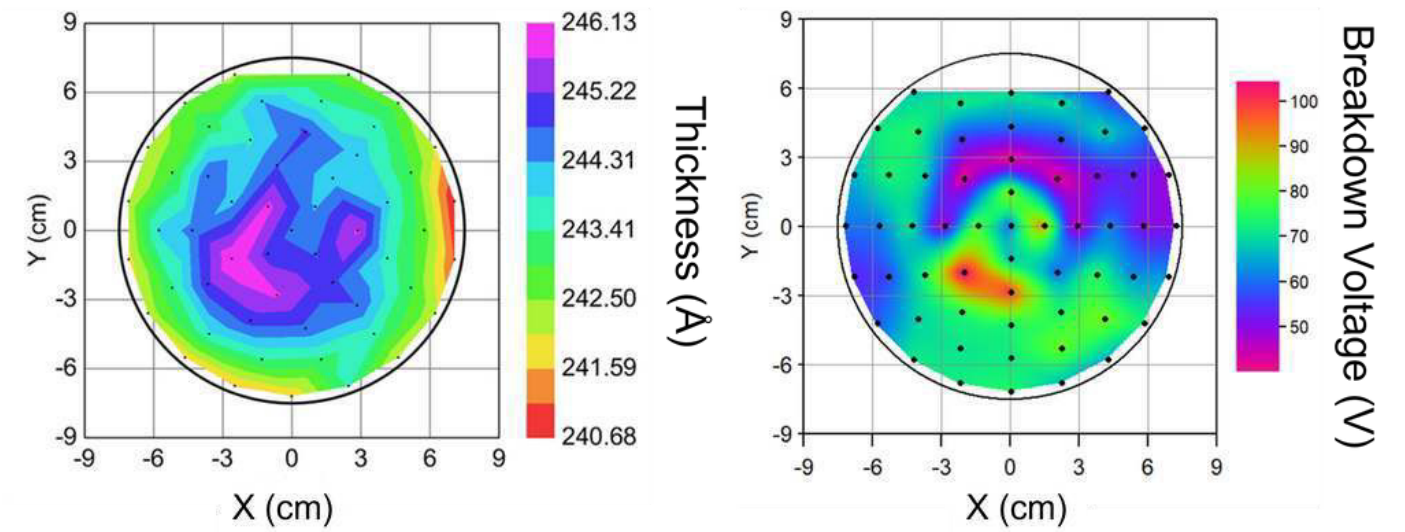

Fig. 4. *Silicon dioxide thin film was prepared by ALD using OI Plasma Technology Atomfab system and subsequently characterized using ellipsometry and nanoTDDB. Left color map shows the thickness distribution of the film and, on the right, the color map shows the dielectric breakdown voltage measured on the same sample. Sample courtesy of OI Plasma Technology.*

Another advantage of AFM instruments is the possibility to characterize sample properties other than topography. For example, nanoscale time dependent dielectric breakdown (nanoTDDB) is a technique that measures the dielectric breakdown of materials. The nanoTDDB technique can be used to perform quality control of freshly deposited dielectric materials prepared by ALD.. Often times, the ALD process needs to be finetuned to produce repeatable results and AFM can provide diagnostic data about the quality of prepared films. In Figure 4, silicon dioxide film was prepared by ALD and its thickness across the entire wafer was measured by ellipsometry. Since some film thickness variation was observed at different positions on the wafer, nanoTDDB was performed to verify the dielectric quality of the film. A correlation between the thinner film thicknesses and lower dielectric breakdown voltages was observed.

Thanks to the small area (tens of nm) that can be probed using nanoTDDB, the sample characterization was more detailed than what would have been possible with bulk TDDB experiments.

Subtle variations and errors in doping levels, mask and implant alignment, and device failures can also be detected using AFM. Specifically, scanning capacitance microscopy (SCM) is an AFM technique which uses a microwave radio frequency (RF) signal to measure the sample's free carrier concentrations and types (electrons n or holes p) as well as the sample's capacitance. SCM data in Figure 5 shows a 30 μm region of static random-access memory (SRAM). The visible structures are transistor devices as seen from the top down, where the metal layering has been removed, along with other features, until just the silicon is exposed. Besides topography, variation in doping levels and dopant type are clearly distinguished in the SRAM sample.

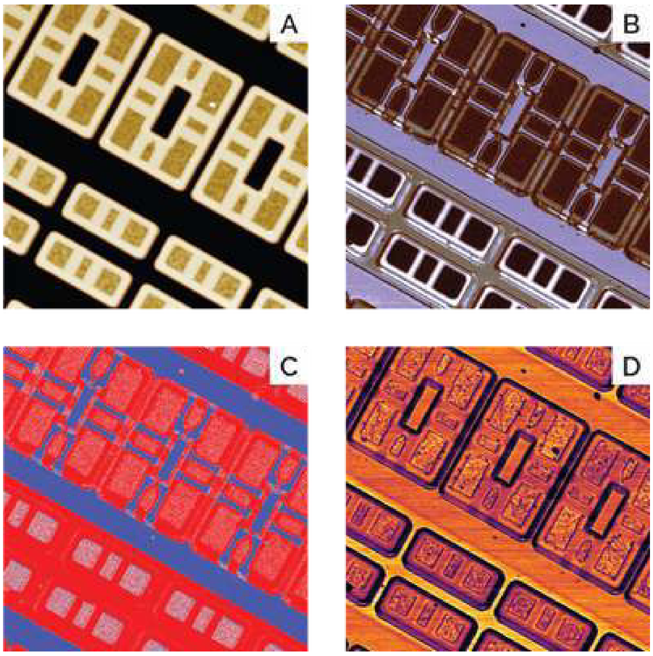

Fig. 5. *SRAM sample with top down access to the source, drain, and gates. All of the channels shown were acquired simultaneously and include a) Topography, b) dC/dV Amplitude where brighter areas indicate lower doping and darker indicate higher doping, c) dC/dV Phase where blue indicates p-type doping and red indicates n-type doping, and d) Capacitance, which has a linear correlation with dopant levels.*

Conclusion

AFM is an indispensable characterization tool for the semiconductor industry as it is the only instrument that can provide reliable 3D surface information such as surface roughness, it is non-destructive, can be used in ambient conditions and requires little or no sample preparation. Furthermore, AFM enables functional measurements which include nanomechanical, nanoelectrical, thermal and other sample properties.

Author's bio

Marta Kocun is a Product Manager at Oxford Instruments Asylum Research, a manufacturer of AFMs. She is responsible for the development of the large sample AFM platform, Jupiter XR.

Interview

Paul Kirby is Senior Marketing Manager at Thermo Fisher Scientific in Hillsboro, Oregon (USA). Paul has worked in a variety of applications and marketing management roles in the semiconductor capital equipment market over the last 4 decades.

How do you see the semiconductor industry coping with current challenges?

Of course, the semiconductor industry is well used to dealing with technology challenges. The challenges of new materials, shrinking line widths, new memory and transistor structures and packaging innovation have been with us for decades. In recent years we have seen inflection points in the number of challenges, as the industry has implemented FinFET and gate all around (GAA) transistors, through silicon vias (TSV's) packaging schemes, 3D NAND memory cells.

These technologies have all driven an increase in volumes of metrology and failure analysis samples and also an increase in the resolution and precision of the analysis tools required to perform the analysis. The resolution requirements have outstripped the capabilities of SEM technology which has led to a gradual increase in volumes of S/TEM samples, for R&D, device characterization, metrology and defect analysis. In addition, the defect localization technologies and sample preparation requirements have also had to keep pace with the roadmap for increased analytical precision.

Focused Ion Beam (FIB) has now become an enabler of the following key semiconductor characterization and metrology workflows:

1. S/TEM Workflows
FIB Sample Delayering -> Electrical Failure Localization -> FIB Sample Preparation -> S/TEM -> Atomic resolution answers

2. SEM metrology workflows with 3D insight
FIB Sample Preparation -> SEM or S/TEM answers

3. Circuit Edit
FIB cut and deposition -> Electrical Test

4. Advanced (2.5D and 3D) Packaging
Electrical Test or Thermal Defect Localization -> FIB Sample Preparation -> SEM answers

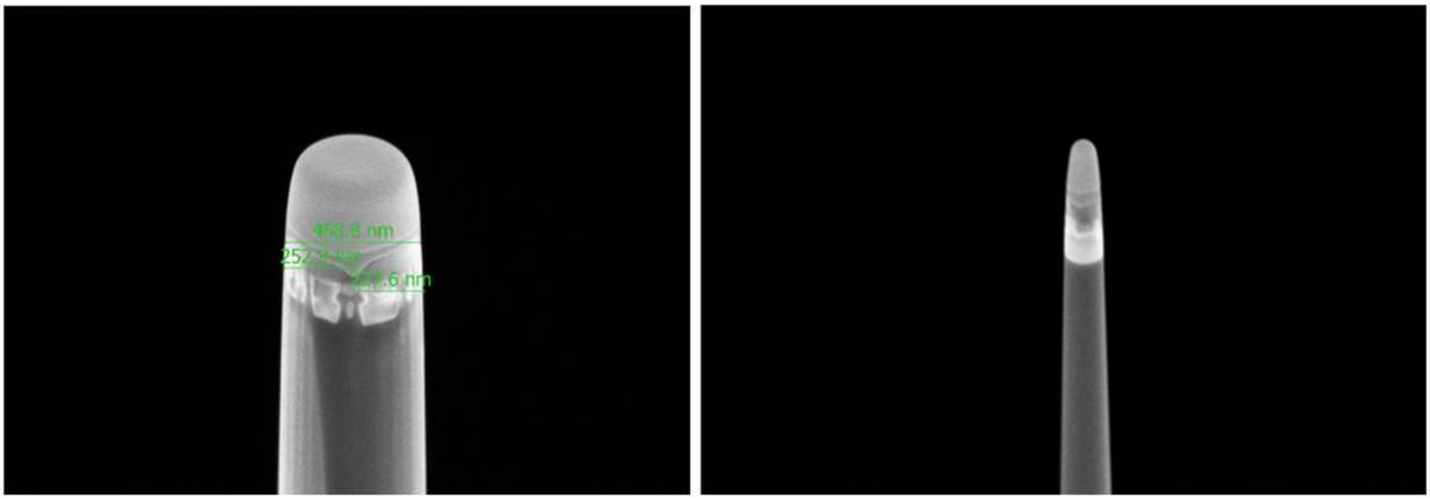

Fig. 1 : *Specific logic gates at geometries of only a few nanometers in width captured with Thermo Scientific Helios 5 FX prepared Atom Probe Tomography (APT) samples.*

The utility of semiconductor characterization techniques continues to grow with the industry requirements for smaller device geometry, atomically smooth surfaces and interfaces, and increased material purity. In your opinion, what are the best and most promising technologies?

Our lives are increasingly dependent on highly complex semiconductor devices. These devices must deliver consistent, repeatable performance as they are the foundation of almost every aspect of our day to day lives. This performance and reliability can only be delivered by devices which have been thoroughly characterized and optimized at the atomic level. The material interfaces, grain orientation, strain, structural metrology, defectivity and stoichiometry must all be characterized and monitored during manufacturing.

A single defect in any of these areas can cause catastrophic device failure. While there are well established (often “top-down” SEM-based) fab processes that can monitor the manufacturing processes, they reached the limits of what they could see about seven years ago, with the transition to FinFET based logic transistors and 3D NAND memory storage cells. S/TEM based workflows are now the process of record to provide the reference data, and actual insight into the complexities of today’s semiconductors. In some cases, Atom Probe Tomography(APT) is also used in conjunction with S/TEM to provide additional atomic chemical analysis, however the success rate and complexity of getting data from Atom Probe samples limits its application for high volume characterization. Both S/TEM and APT workflows now absolutely require Focused Ion Beam (FIB) to create the highest quality, precise, site-specific samples at increasingly high volumes.

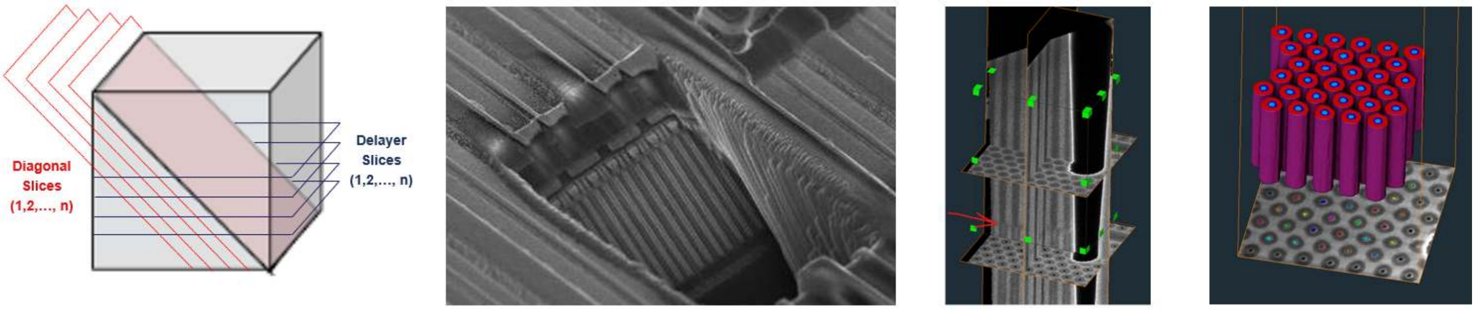

Fig. 2 : *3D reconstruction for nanometer resolution metrology and defect analysis of 3D NAND structures generated from thin slice images. Images are produced with the Thermo Scientific Helios 5 PXL delayering or diagonal mill capabilities and Thermo Scientific Avizo Software.*

Is SEM characterization of semiconductors "dead"? No, SEM can still provide rapid, high-resolution answers to fab metrology challenges, however it cannot easily measure buried features or characterize 3D structures which are now pervasive in most semiconductors. X-ray and other techniques continue to be investigated, but they are either too costly or too slow to proliferate widely. The most important trend that we see is the increasing use of (Xe) FIB technology to perform high speed cross sectioning or delayering to expose the region of interest prior to SEM metrology or defect inspection in the wafer fab. This provides deep 3D insight into the manufacturing processes in the fastest possible time. The combination of FIB and sub-nm resolution SEM means that high resolution cross section or 3D reconstructed data sets can be created to support the high-volume manufacturing of logic, memory, power, analog/mixed signal, and display devices.

Another driver for the adoption of high-volume FIB analysis is Circuit Edit (CE) or circuit modification. As mask costs have sky-rocketed with each successive technology node, the semiconductor device manufactures now fundamentally rely on using a high precision FIB beam to surgically cut circuit connections or deposit insulating and conductive material to rapidly reconfigure circuits and adjust the device performance. This eliminates costly mask modifications and re-processing.

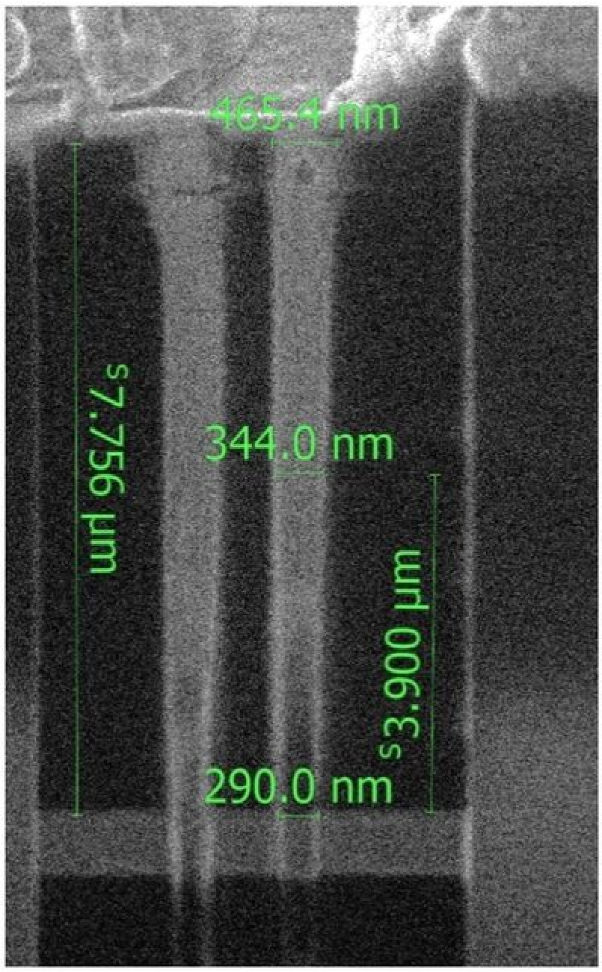

Fig. 3 : *Circuit edited interconnects with a 20:1 aspect ratio and 300nm diameter enabling fast device prototyping, debug and repair.*

Why are FIB applications becoming pervasive in the fields of semiconductor metrology, analysis and characterization?

FIB provides several unique capabilities to semi manufacturers. Some of these applications are used in relatively low volume and in either a manual or semi-automated workflow, for example CE. But increasingly there is the need to fully automated, high volume FIB applications, two of which are outlined below.

A FIB can remove material with extreme precision, routinely creating samples for S/TEM or APT as outlined previously. It can create samples less than 20nm thick that may be site specific and end-pointed at a specific defect location. FIB's can also be programmed to make samples at repeated locations on semiconductor wafers to provide routine checking and metrology answers in high volume. These S/TEM sample preparation workflows are now the most common application for FIB and are pervasive at all the major manufacturers and foundries. The semiconductor industry roadmap now fundamentally relies on the continued development of automation and repeatability in this area.

The other automated FIB application that is becoming adopted at increasingly high rates is in fab SEM metrology, where the FIB can expose buried structures, either by delayering, diagonal cut or cross section which can then be measured with the in situ, sub-nm resolution SEM.

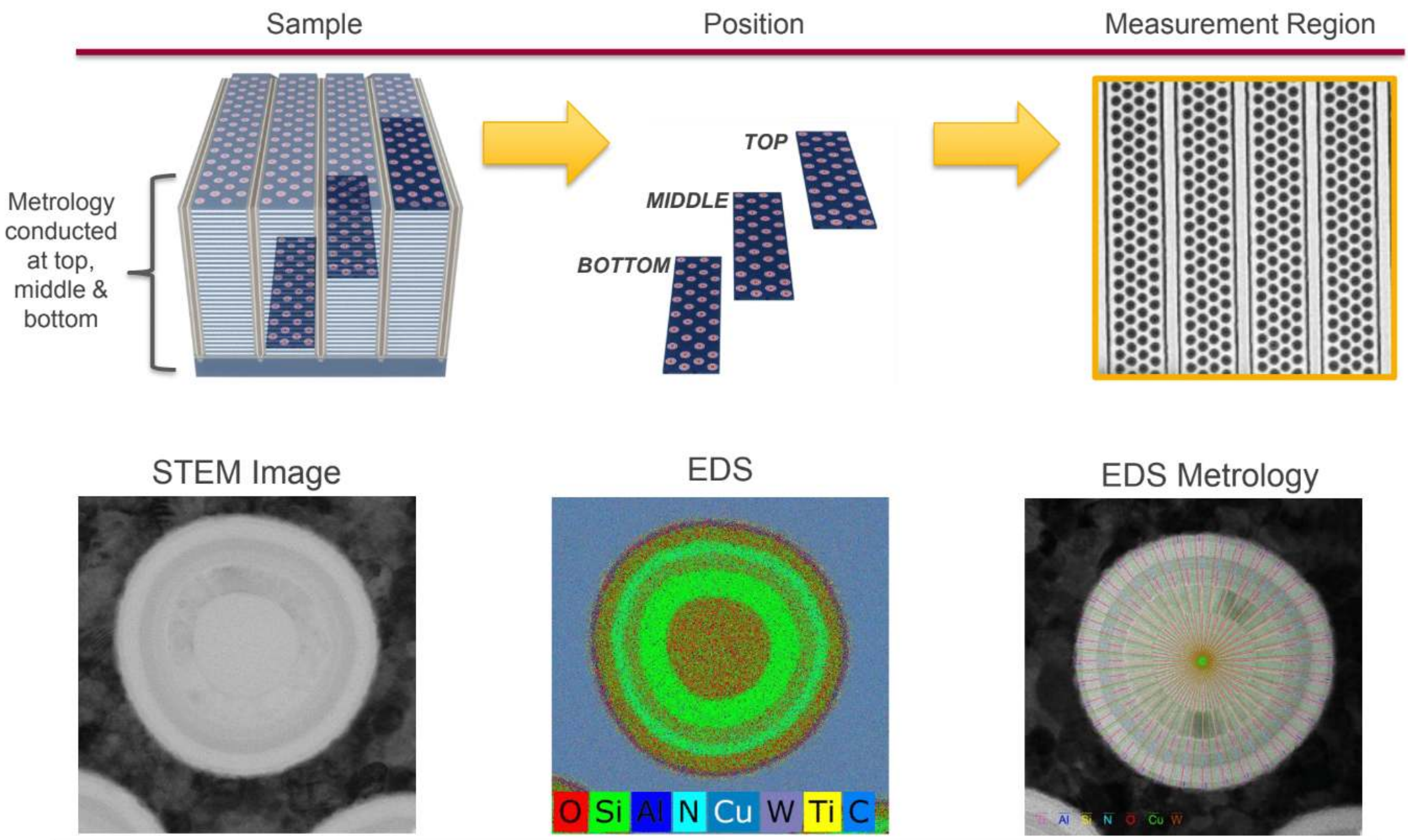

Fig. 4 : *Automated, site-specific, FIB sample preparation enables high quality sub-nm resolution, STEM metrology and EDS analysis workflows.*

Can you give an example of a key application?

While we have mentioned many of the high-volume applications for FIB in the previous paragraph, one of the most recent growth applications that we see is failure analysis of semiconductor devices which include advanced packaging technology. These devices incorporate 3D stacked die with through silicon via (TSV) interconnects. The package may include multiple die of the same type or heterogeneous integration of many types of die. In either case, the failure analysis(FA) challenges they introduce are significant. Once you have isolated the potential location of the defect in 3D space, using techniques such as Lock in Thermography (LIT), the FA engineer now needs to get access to a region of interest(ROI), which may be only 10's of nm's in size in many cubic mm's of material before they can perform their SEM or TEM analysis.

The latest generation of Xenon (Xe) Plasma FIB (PFIB) systems provides the answer. They can remove large volumes of material without creating unwanted damage in the device itself. This may still take several hours of milling to access the ROI, so the latest FIB systems for advanced packaging now incorporate in-situ femto-second lasers to assist with the high-volume material removal. A combination of laser in conjunction with Xe PFIB for the final cleaning polish can provide extremely high-quality SEM cross section results in the shortest possible time, enabling engineers to rapidly characterize and resolve manufacturing defects.

How do you see the current technology evolving with current resource and geopolitical challenges?

The pace of innovation is not slowing down. The requirement for atomic resolution characterization is only becoming more important. FIB sample preparation is a fundamental enabling technology for these workflows. For many years these workflows have relied on the skills of talented engineers, technicians and operators, but these resources can no longer scale up to meet the growing needs of the semiconductor market. While manual FIB processing of critical samples will continue, there are an increasing number of FIB workflows which can now be (and are being) highly automated with the incorporation of Artificial Intelligence (AI).

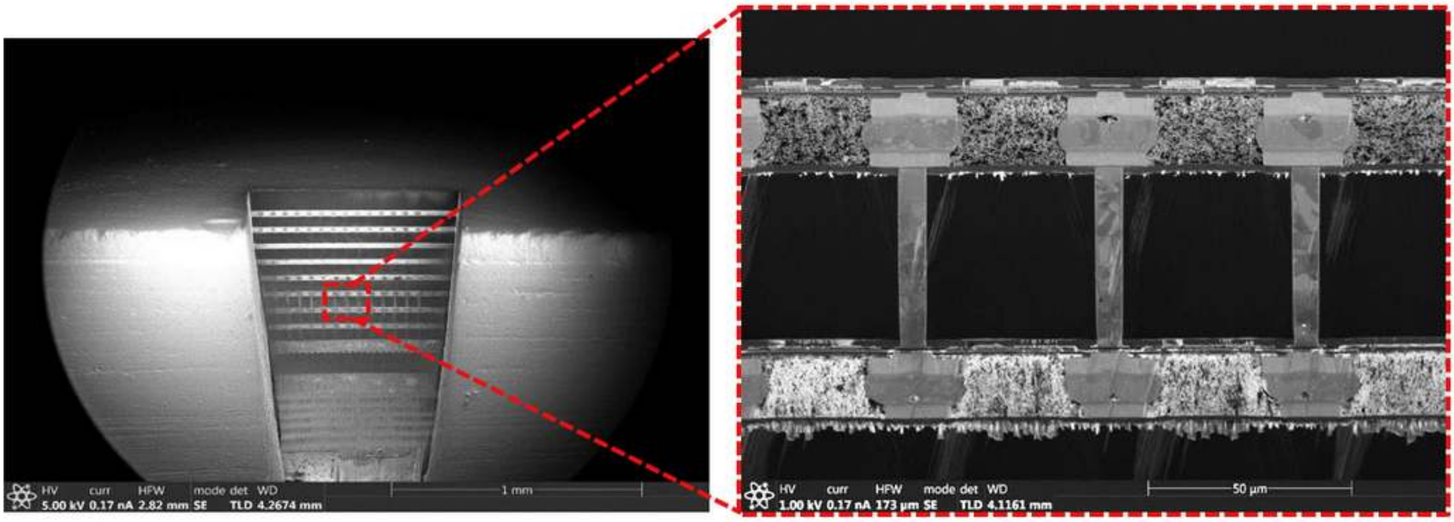

Fig. 5 : *High resolution "curtain free" SEM images in large volume 3D packaged semiconductor device acquired with in-situ laser ablation and PFIB polishing enabled by the Thermo Scientific Helios 5 Laser PFIB.*

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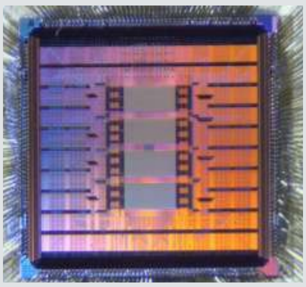


NIST and Google to Create New Supply of Chips for Researchers and Tech Startups

The chips will be manufactured by SkyWater Technology at its Bloomington, Minnesota, semiconductor foundry. Google will pay the initial cost of setting up production and will subsidize the first production run. Read more

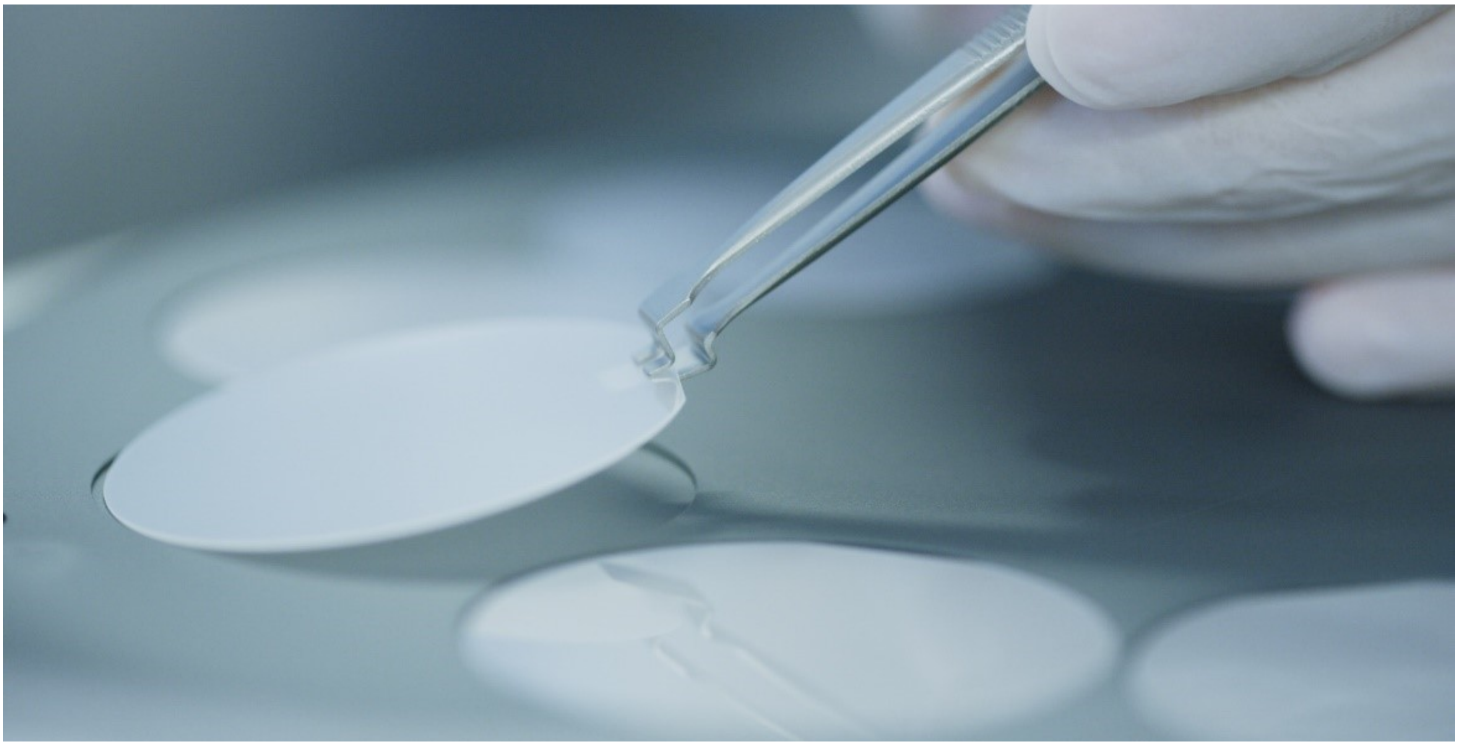
The emergence of UV-C LED industry and the impact of graphene and nanowire hybrid technology in semiconductor

In this article, CrayoNano, a Norwegian semiconductor company specializing in nanomaterial-based semiconductor technology, introduces a novel approach using AlGaN-based nanowires in the manufacturing of UV-C LEDs – the results are strain and stress-free crystals and reduction of threading dislocations. The advantages of this approach addresses the challenges in conventional AlGaN-based thin-film UV-C LED technology for commercialization.

UV-C light has the incredible ability to kill 99.9% of bacteria and viruses in seconds. The short wavelength of the UV-C range, 100 nm–280 nm, creates sufficient energy to neutralize pathogens by creating photochemical changes in their DNA, impairing their ability to reproduce. UV-C light as a disinfection method is being increasingly applied to mainstream solutions, such as food packaging, surface, air, and water disinfection.
Today, mercury vapor lamps and chemical cleaning are the main modes of disinfection. Mercury vapor lamps are the easiest and most well-known way of producing UV-C light, dominating the majority of UV-C markets. However, mercury lamps contain vaporized mercury which is toxic to humans. Industrial and commercial chemical cleaning – such as chlorine used in water treatment – is one of the easiest and accessible methods of disinfection. However it is extremely labor intensive and the effects of human exposure to chemicals is a major risk and concern. Better alternatives and solutions for effective and automized disinfection is needed.

The mercury-free and non-toxic AlGaN semiconductor-based UV-C light emitting diodes are rapidly progressing due to the increasing demands for disinfection. The global estimated UV-C LED market size was valued at 460 USD million in 2021 and is projected to reach 2.5 billion by 2026, registering a CAGR of 40 %. Mercury lamps and chemicals are vastly being used and may always be around. The strong growth potential of UV-C LED technology can be unleashed by significant improvement of cost performance and production scaling. Today's market leaders are based on thin-film technology that has intrinsic challenges of dislocation densities, heat extraction, and internal polarization, thus leading to limited performance and cost efficiencies.

The revolutionary approach to producing UV-C LEDs based on the use of low-dimensional, nanomaterials as a substrate and nanowires for the UV-C LED heterostructure, targets to overcome the existing major challenges of thin-film UV-C LED technology.



CrayoNano grows AlGaN nanowires UV-C LEDs to create an energy efficient and high performing semiconductor chip.

Challenges with current available UV-C LED technology

State-of-the-art thin-film UV-C LEDs are manufactured in conventional planar heterostructures of group III-nitrides, as shown in Figure 1. The main issues with thin-film UV-C LEDs stem from the growth of these layered heterostructures on a substrate with a large lattice mismatch. The of the device, reduce light emission and trap heat, which results in impaired device performance (reflected in low wall plug efficiency of 1-5%), reduced lifetime (1,000-10,000h), as well as struggling to manufacture at high volumes due to low product yield (5-20%). Additionally, the layering process is time-intensive, has a high equipment capital expenditure, and is costly due to the sheer amount of expensive AlGaN and AlN material used to overcome defect issues.

When using conventional thin-film production methods, it is not possible to simply reduce the number or thickness of the AlN and AlGaN layers because of lattice mismatch. Furthermore, the stress inherent to thin films limits the scalability of the technology, and commercial volume production is currently standing still at 2-inch wafers based on available market information.

Most UV-C LEDs are grown on sapphire substrates, as shown in Figure 1, where the relatively large lattice mismatch of 14% between sapphire and AlN results in the formation of various defects at the interface. Among these defects, threading dislocations and point defects are the main causes of poor crystal quality leading to structural failure, reduced internal quantum efficiency, and low production yields, limiting volume production capacity.

Many approaches have been explored to produce low threading dislocation density (TDD) AlN on sapphire templates. With extensive efforts, TDDs in the range of $10^7 – 10^8$ cm^{-2} are demonstrated, which is still considered high. Single-crystal AlN templates obtained from bulk AlN showed a reduced TDD as low as $10^2 – 10^3$ cm^{-2}. However, these templates are expensive and significantly decrease the cost efficiency of produced UV-C LEDs, affecting business profitability. While the quality of AlN has dramatically improved over the years, there has been a continuous quest to seek technology or materials which can overcome this challenge.

Another issue with conventional UV-C LEDs is the necessity for highly conductive n-AlGaN current spreading layers for lateral current injection, as sapphire and AlN are electrically insulating. This makes the efficient n-doping of AlGaN critical for low-voltage operation. However, at higher Al-composition of AlGaN, n-doping becomes inefficient, and the layer becomes highly resistive. Therefore, an alternative highly conductive current spreading layer below the n-AlGaN layer could be a potential solution for efficient lateral electron injection.

In summary, the main challenges of current technologies are:
• Struggle to scale to high volume manufacturing
• Low wall plug efficiency (WPE)
• Low output power
• Reduced operating lifetime

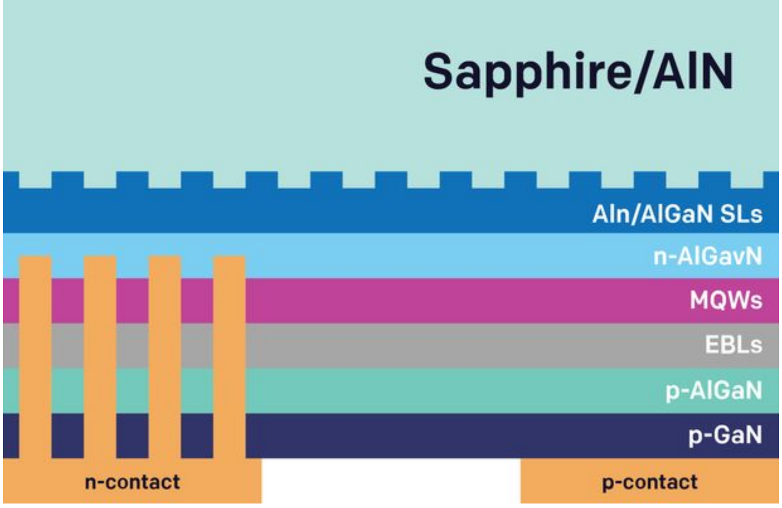


Fig.1: *Simplified graphic illustration of a conventional thin-film UV-C LED. (Source: CrayoNano)*

CrayoNano's graphene –nanowire hybrid-based UV-C LEDs can overcome the challenges of thin-film technology

The described novel approach of CrayoNano originates of early stage research at Norwegian University of Science and Technology (NTNU) that had been matured by CrayoNano, targets to overcome the intrinsic challenges in AlGaN-based UV-C LEDs by epitaxially growing AlGaN nanowires on top of graphene substrates, as shown in Figure 2. Graphene possesses outstanding properties of high thermal conductivity, and high transparency to the light of all wavelengths, combined with a low sheet resistance. With graphene's high conductivity, the graphene substrate also becomes the n-side electrical contact and an efficient current spreader layer without absorbing UV-C light coming from the active region of the LED. Moreover, the graphene layer may provide better thermal management because of its high thermal conductivity.

This revolutionary approach to produce UV-C LEDs circumvents the issue of lattice mismatch by growing perfectly crystalline AlGaN nanowires on a graphene film. This enables dislocation-free devices with semi-polar orientation to achieve higher internal quantum efficiency compared to thin-film technology. The precision-engineered nanowire growth technology further minimizes the amount of expensive AlGaN material used, while simultaneously enhancing the device's overall performance.

In summary, this technology is able to scale into volume, high yields, higher efficiency and lower internal heat generation: LEDs emit more light and less heat. The high crystal quality of each nanowire will, in turn, improve wafer quality and production yields, breaking through the capacity limit of current UV-C LED manufacturing processes. Technology scaling and high-volume production drives competitive cost-performance, resulting in the potential not just to replace existing thin-film UV-C LEDs, outcompete mercury lamps, and ultimately opening access to compete chemical cleaning in the future. Compared to currently available UV-C LEDs, these nanowire LEDs have the potential of:

• **Scalable technology optimized for high volume manufacturing:** Because of their high strain-tolerance our nanowires do not have threading dislocations nor cracking or other propagating defects related to larger areas.

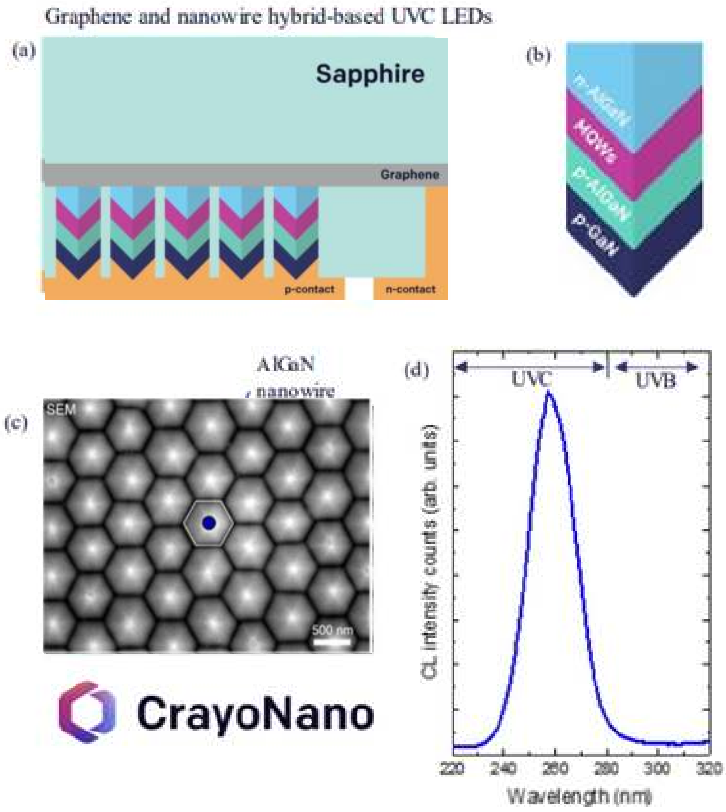


Fig.2: *Graphene and nanowire hybrids based UV-C LEDs. Simplified graphic illustration of (a) CrayoNano's nanowire on graphene UV-C LED design, and (b) Heterostructure of an individual nanowire. (c) Top-view SEM of AlGaN nanowires on graphene. (d) Cathodoluminescence spectrum of an individual nanowire with the emission in UV-C range which can be tuned to the desired wavelength by varying Al-composition of the AlGaN active layers. (Source: CrayoNano)*

This in turn enables larger wafer sizes and higher yields. Additionally, low temperature processes can be used to utilize existing and available equipment. Together this will lead to the capability to deliver in high volumes in the hundreds millions of units.

• **Higher wall plug efficiency (WPE):** Growing AlGaN semiconductor material in the form of dislocation-free nanowires on graphene rather than planar layers leads to potentially better light extraction and higher internal quantum efficiency.

As a result, nanowire LEDs will emit significantly more light with a possibility to reach a WPE greater than 30%, compared to just 1-5% of today's thin-film UV-C LEDs.

• **Less heat generation:** With good heat dissipation through the graphene layer, nanowire LEDs will produce less internal heating than standard UV-C LEDs. This significant reduction in the energy conversion into heat will directly increase the device's lifetime.

• **Longer operating lifetime**: Nanowires are more strain-tolerant than the thick layers of semiconductor material and buffer layers in the thin-film planar design. This makes LEDs better equipped to absorb strain and decreases the concentration of defects in the final product leading to a slower decrease in performance with operation time. With this design, nanowire LEDs on graphene have the potential to reach a lifetime of 25000 hrs.

• **Outperforming price performance**: Expensive AlN substrates and buffers consisting of thick planar layers used in standard UV-C LEDs are avoided. Reducing the number of layers and their thickness, enabling process scalability, and taking advantage of a well-established supply chain will increase production capacities, efficient processing, and reduce materials costs. These cost savings, together with operating life beyond 25,000 hours, represent the potential to reach single-digit US dollar/Watt values in the next five years from this new technology compared to standard thin-film UV-C LEDs.

Innovative technology enabling a healthier and sustainable future for everyone

Considering the exponential increase in the demand for disinfection technology, there is an urgent need for safe, environmentally friendly, cost-efficient, and available semiconductor-based UV-C LEDs to outperform many UV-C mercury-based lamps and chemicals in the market. Although technological solutions offered by conventional thin-film UV-C LEDs are making steady advancements, progress is relatively slow; the low cost efficiency of existing products makes it difficult to compete with existing mercury lamp solutions and chemical cleaning. This new technology offers a next-generation semiconductor solution to overcome the performance challenges of thin-film UV-C technology, leading to an outperforming product meeting disinfection requirements and automized solutions for a healthier and sustainable life.

CrayoNano is a global semiconductor component manufacturer enabling a sustainable and healthier life for everyone through market-influencing photonic device technologies. With groundbreaking, patented technology of merging two nanomaterials, the first application is a graphene-nanowire hybrid, energy efficient UV-C LED ideal for water, air and surface disinfection. Its strong global patent portfolio covers all major aspects of the company's technology – including semiconductor epitaxial growth and processes, nanomaterials and nano-structuring, package and assembling technologies, and devices. The continued IP generation targets the key commercial aspects and hurdles of the semiconductor process, enabling the commercialization of its customers solutions and new technologies for new applications to reach the market potential.

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MXenes: nanometer-thick metals for semiconductor industry

Hyunho Kim [1] Babak Anasori, [2], [3] Yury Gogotsi [1]*

[1] A. J. Drexel Nanomaterials Institute and Department of Materials Science and Engineering, Drexel University, Philadelphia, PA 19104, United States
[2] Department of Mechanical and Energy Engineering, and Integrated Nanosystems Development Institute (INDI), Purdue School of Engineering and Technology, Indiana University-Purdue University Indianapolis, IN 46202, United States
[3] School of Materials Engineering, Purdue University, West Lafayette, Indiana 47907, USA
* e-mail: gogotsi@drexel.edu

Introduction: What are MXenes?

MXenes are two-dimensional (2D) transition metal carbides, nitrides, and carbonitrides, which were first reported in 2011 and have become one of the largest and the fastest growing 2D material family, offering a wide selection of atomic structures and compositions, hence tunable optical, electronic and chemical properties.[1] Most MXenes can be synthesized from the layered ternary carbides and nitrides (so-called MAX phases) precursors, with a unit formula $M_{n+1}AX_n$, where M represents an early transition metal (Ti, V, Nb, Mo, etc), A is a group IIIA-IVA element in the periodic table (typically, Al), X is C and/or N, and n=1 – 4 (Figure 1). By selective chemical etching of the 'A-element' layers and subsequent delamination, the freestanding (sub)nanometer-thin $M_{n+1}X_n$ sheets can be obtained with surface functional groups (T_x).

MXenes are thus described with a formula of $M_{n+1}X_nT_x$. While the core MX compositions of MXenes are determined by the precursor composition, the surface functional groups can be controlled mainly by the synthesis route, the choice of etchant and post-processing. The terminations are mainly oxygen, hydroxyl, and fluorine for the aqueous acid etching route, and chalcogens and halogens terminations are available when molten salt etching is used. The presence of surface functional groups allows MXenes to possess both high electrical conductivity and hydrophilic surface at the same time. Hydrophilicity of MXenes allow their processing into films and devices by spin coating, 2D and 3D printing from aqueous solutions with no surfactant or binder. For instance, $Ti_3C_2T_x$, the most studied MXene, has been reported with electrical conductivity of up to 25,000 S/cm,[2] which is the highest electrical

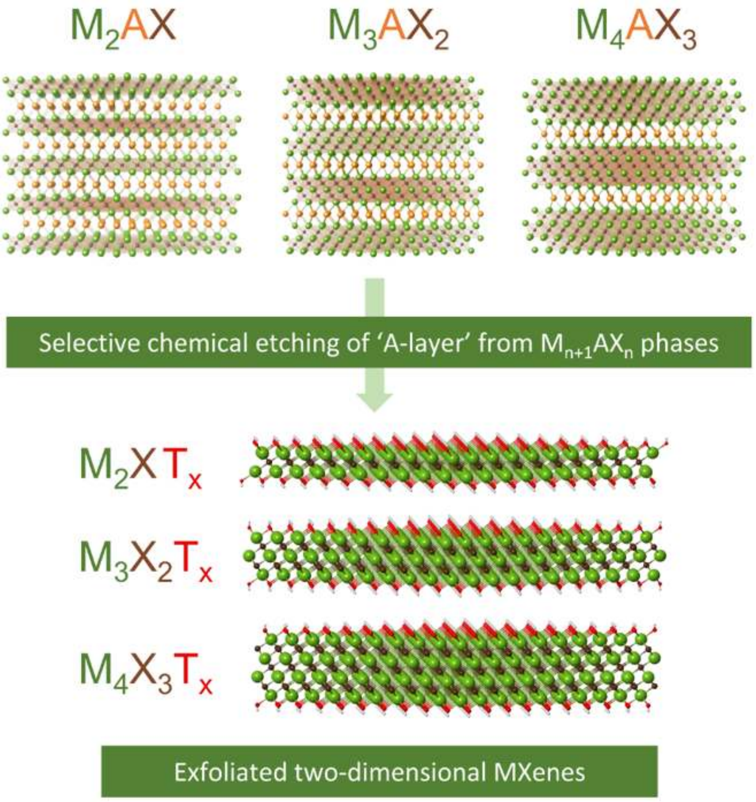


Fig. 1. *Schematic illustration of the most common atomic structures of typical MAX phase and MXenes (n=1-3). Green, orange, brown, and red color balls represent transition metal (M), group-A elements (A), carbon/nitrogen (X) and surface functional groups (Tx), respectively.*

conductivity among all solution-processed nanomaterials. However, the conductivity values can vary within 4 orders of magnitude, depending on the number of atomic layers, M and X elements and surface terminations of MXenes. Additionally, a 1-nm-thick sheet of $Ti_3C_2T_x$ MXene has the breakdown current density 1.2 x 10^8 A/cm² [3], which exceeds that of copper and other conventional metals and makes MXenes promising for nanometer-thick interconnects. MXenes' unique properties combination (functionalizable surfaces, plasmon resonances from UV to IR range, metallic character of conductivity, with a high density of states at the Fermi level, high concentration of carriers, etc.) combined with their 2D morphology and ease of large-scale manufacturing promise high performances in various fields, including energy storage [4], electromagnetic interference (EMI) shielding [5] , communication, plasmonics and photonics, catalysis [6], and sensors [7, 8]. The potential of MXene in semiconductor industry is discussed in following sections, based on the great processability and scalability of MXenes and a wide range of work functions, which exceeds that of conventional metals. These advantages make MXenes promising for van der Waals metal-semiconductor interconnects, electron and hole transport layers, transparent and flexible printable electrodes. etc.

Processability: Solution processing and scalability

The multilayer MXene can be exfoliated via solution-processing into single- and few-layer 2D flakes by intercalation of cations followed by shaking or sonication with repeated washing. The ion intercalation/exchange between the MXene layers and the co-intercalation of water molecules decrease the adhesion between adjunct nanosheets, resulting in spontaneous delamination.

The negative surface charge (zeta potential from -30 to -80 mV) of MXenes with their 2D morphology introduces a strong relationship between the concentration and the rheological properties of MXene dispersion, offering a wide choice of processing methods (summarized in Figure 2). The higher concentration dispersion shows the viscoelastic behavior of gel or liquid crystal [9]. Water-based stable colloidal suspension of MXene flakes without additives can be used as conductive MXene inks [10]. Additionally, inks with different solvents can be easily fabricated, thanks to the dispersibility of MXenes in polar organic solvents [11].

Using MXene inks, transparent, flexible, and conducting MXene thin films can be deposited by using common deposition methods, such as printing, spin coating, and spray coating. Vacuum-assisted filtration can offer thicker freestanding MXene “paper”. Mayer bar, doctor blade, or slot-die coating are suitable for the continuous roll-to-roll processing of thick MXene films. For patterned deposition, inkjet printing or screen printing can be considered for low or high-viscosity dispersions (inks), respectively. In addition, layer-by-layer deposition method is available, benefitting from the negative surface charge of MXene. Liquid-liquid interface assembly method can form an ultrathin film, down to a monolayer, with maximized coverage [12].

MXenes can also be processed into fibers by wet spinning of concentrated liquid-crystalline dispersions [13], which is promising for flexible and wearable device applications.

MXenes can also be dispersed in polar organic solvents, including ethanol, dimethylformamide (DMF), dimethyl sulfoxide (DMSO) and n-methyl-2-pyrrolidone (NMP). The organic dispersion can be considered for MXene coating on water-sensitive materials or for extended shelf life. Surface treatment with phosphonic acid can tune MXenes’ surface functionality which eventually allows their dispersion in non-polar organic solvents, including chloroform and hexanol [14].

Impact: Potential for applications in semiconductor industry

MXenes can be considered as 2D metals and can be used as nanometer-thick building blocks for manufacturing conducting electrodes and interfacial layers which make electrical contact with the semiconductor layer. First, MXene can offer a wide range of work functions by varying MXene composition and/or surface functional groups. Theoretical studies have predicted ultralow work function of 1.6 eV for OH-terminated Sc_2C MXenes [15]. The intrinsic dipole moments of hydroxyl groups are the main cause of ultralow work function.

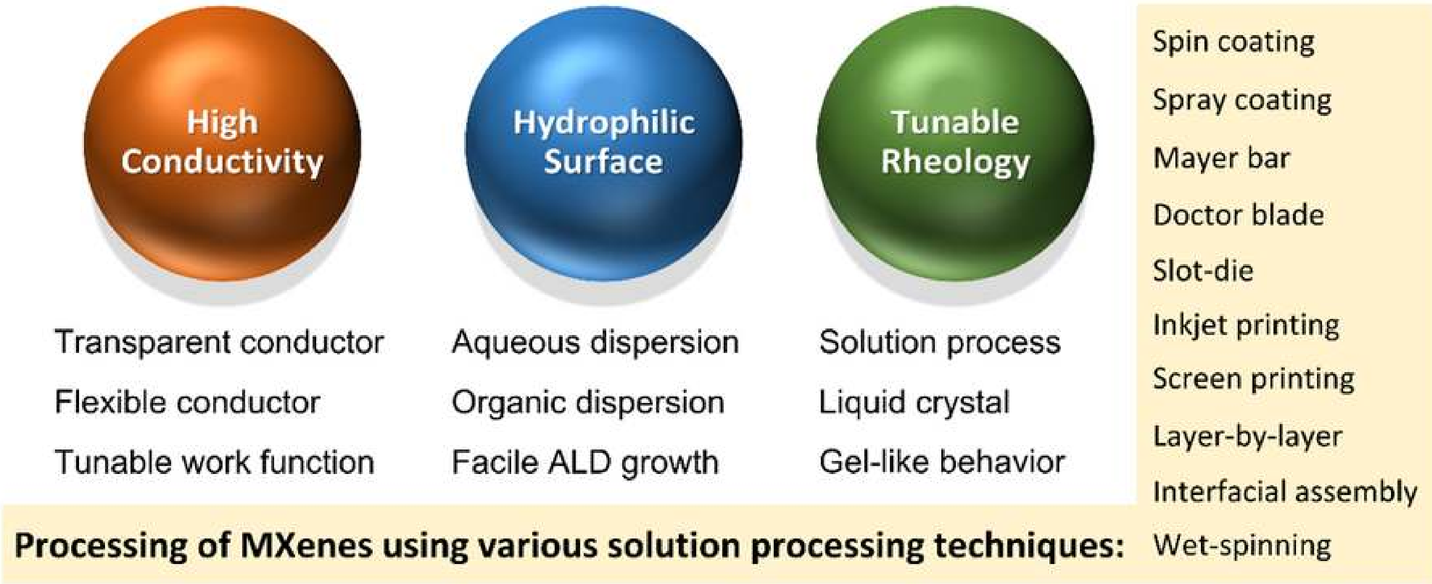


Fig. 2. Schematic presenting advantages of MXenes and listing various solution processing techniques.

On the other hand, O-terminated V2C MXene is expected to have a large work function of 6.7 eV [15]. These extreme work function values are not available from conventional metals, making MXenes strategic building blocks for microelectronics. MXenes can be deposited by solution-processing where the underlying semiconductor material is not likely to be damaged. High-energy deposition, such as electron-beam evaporation or sputtering of metals, may result in unwanted penetration of metal atoms into underlying semiconductor and Fermi-level pinning at the metal-semiconductor interface [16]. In contrast, transferred metal contacts have demonstrated nearly Schottky-Mott limit in van der Waals metal-semiconductor junction [16]. Solution-processed MXene thin films are most likely to form a van der Waals contact which has a potential for engineering a Schottky barrier height and realization of ultralow contact resistance.

In addition, the hydrophilic surface of MXene offers great compatibility for material growth. For instance, atomic layer deposition (ALD) can be directly used on MXene thin films [17]. while the same is challenging on graphene. Moreover, the hexagonal atomic arrangement of MXene surface can be used for epitaxial growth; e.g., (111)-oriented $BaTiO_3$ film and GaN nanowires have been demonstrated [18, 19].

MXenes have shown great potential in the field of optoelectronics and plasmonics. $Ti_3C_2T_x$ MXene significantly improved the perovskite solar cell efficiency when utilized as an interfacial layer next to the perovskite and as electron transport layer, as well as a dopant for perovskite [20]. Spin-coated $Ti_3C_2T_x$ MXene improved responsivity and quantum efficiency of a gallium arsenide (GaAs) photodetector compared to the gold contacted counterpart [21]. MXenes have also been for use in photocatalysts by assembling with semiconductor nanoparticle or acting as single atom catalyst host [22, 23].

Beyond the direct use of MXenes, they can also be used as precursor materials to synthesize other 2D structures. For instant, V_2CT_x MXene has been used as a vanadium source for the solvothermal synthesis of metal-organic framework (MOF) [24]. The resulting MOF was found to maintain 2D structure inherited from MXene. It was stable enough for the microfabrication process. Similarly, 2D $KNbO_3$ crystals were formed once Nb_2CT_x MXene was used as a niobium source in hydrothermal oxidation reaction with the presence of surfactant [25]. More than a dozen of MXene-derived functional materials with unique functionalities have been developed.

Another important aspect of MXenes is their biocompatibility. $Ti_3C_2T_x$ and several other MXenes and their hydrogels are known to be safe in contact human skin and as implants. MXene-based epidermal electrodes have shown improved vapor permeability while maintaining low impedance with skin and comparable electro-physiological signal detection to a commercial gold or Ag/AgCl gel electrodes [26].

MXene hydrogels have been used as pressure and motion sensors, which can be coupled with monitoring of pH change in sweat. With the recent development in communication, internet-of-things, and artificial intelligence, MXene can play an important role in epidermal and implantable electronics, shaping the future of healthcare and health monitoring.

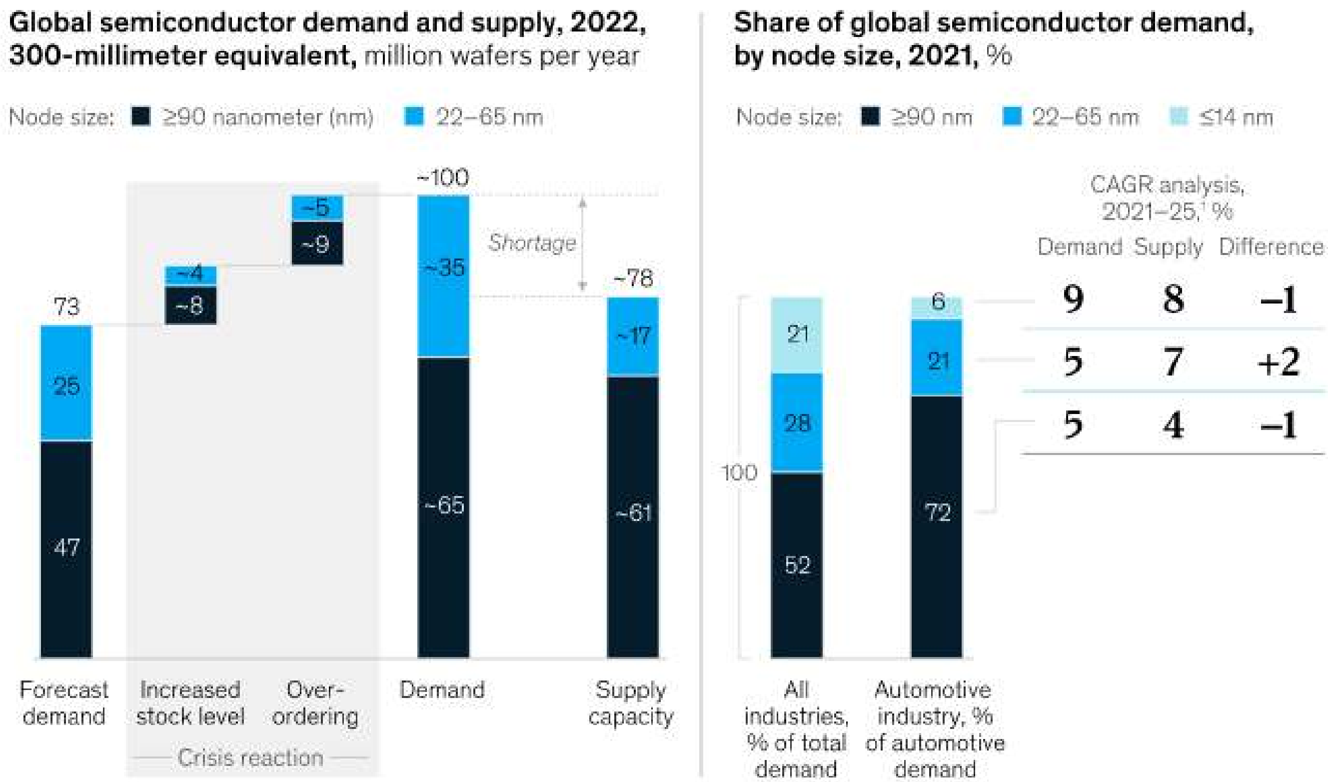
In summary, the unusual combination of metallic conductivity, hydrophilicity, plasmonic properties and other characteristics of MXenes that can be finely tuned by changing structure and surface chemistry may open numerous opportunities for applications in semiconductor industry, in particular, enabling flexible, printable, and transparent devices.

References on page 52

Semiconductor shortage: How the automotive industry can succeed

(McKinsey)

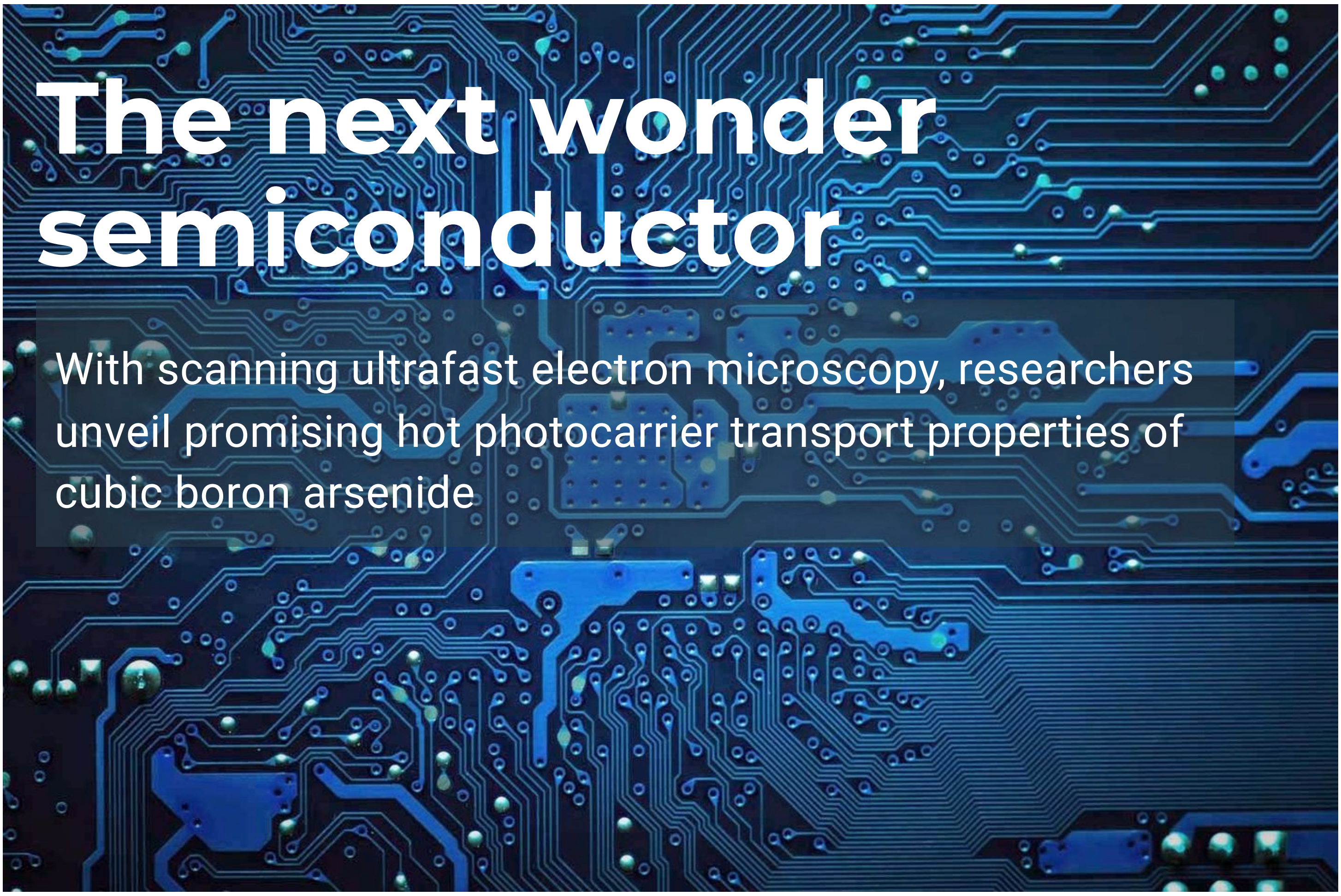
As the semiconductor shortage persists, the automotive industry will likely benefit from new sourcing models and stronger bonds between OEMs, Tier 1 suppliers, and semiconductor suppliers.



For nodes greater than 90 nanometers (nm), which are in high demand in the automotive industry, the shortage is likely to persist for two reasons. First, the semiconductor industry is unlikely to address the structural reasons for this shortage, because mature nodes have low profit margins. Second, some end customers appreciate the attractive price point of mature nodes and have a limited incentive to migrate to lower node sizes, because of the additional development and qualification costs, as well as the limited availability of R&D staff.

For wafers from 22 to 65 nm, the shortage will not fully resolve over the short- to midterm, but it may lessen if semiconductor companies increase their supply, as expected. Overall, however, it is difficult to predict the size of the demand–supply gap for specific products in this group, given the high heterogeneity of device types and technologies.

Read the full report



The next wonder semiconductor

With scanning ultrafast electron microscopy, researchers unveil promising hot photocarrier transport properties of cubic boron arsenide

By Sonia Fernandez
University of California, Santa Barbara

In a study that confirms its promise as the next-generation semiconductor material, UC Santa Barbara researchers have directly visualized the photocarrier transport properties of cubic boron arsenide single crystals.

“We were able to visualize how the charge moves in our sample,” said Bolin Liao, an assistant professor of mechanical engineering in the College of Engineering. Using the only scanning ultrafast electron microscopy (SUEM) setup in operation at a U.S. university, he and his team were able to make “movies” of the generation and transport processes of a photoexcited charge in this relatively little-studied III-V semiconductor material, which has recently been recognized as having extraordinary electrical and thermal properties. In the process, they found another, beneficial property that adds to the material’s potential as the next great semiconductor.

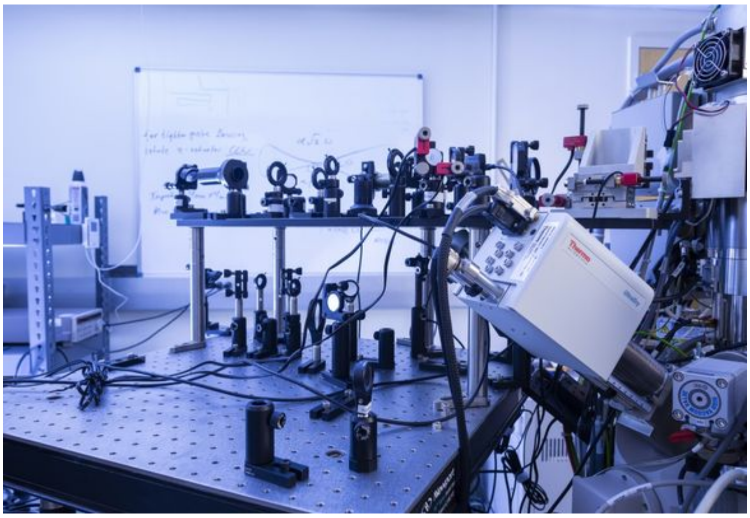
Their research, conducted in collaboration with physics professor Zhifeng Ren’s group at the University of Houston, who specialize in fabricating high-quality single crystals of cubic boron arsenide, appears in the journal Matter.

‘Ringing the Bell’

Boron arsenide is being eyed as a potential candidate to replace silicon, the computer world’s staple semiconductor material, due to its promising performance. For one thing, with an improved charge mobility over silicon, it easily conducts current (electrons and their positively charged counterpart, “holes”). However, unlike silicon, it also conducts heat with ease.

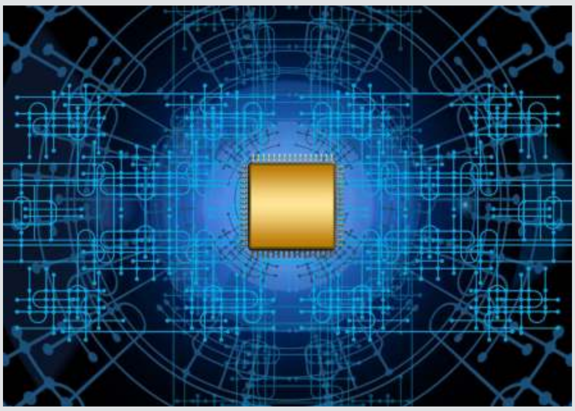
“This material actually has 10 times higher thermal conductivity than silicon,” Liao said. This heat conducting — and releasing — ability is particularly important as electronic components become smaller and more densely packed, and pooled heat threatens the devices’ performance, he explained.

“As your cellphones become more powerful, you want to be able to dissipate the heat, otherwise you have efficiency and safety issues,” he said. “Thermal management has been a challenge for a lot of microelectronic devices.”



The scanning ultrafast electron microscope (SUEM) couples a femtosecond pulsed laser with a scanning electron microscope, which enables time-resolved imaging of microscopic energy transport processes with simultaneously high spatial and temporal resolutions. @ MATT PERKO

What gives rise to the high thermal conductivity of this material, it turns out, can also lead to interesting transport properties of photocarriers, which are the charges excited by light, for example, in a solar cell. If experimentally verified, this would indicate that cubic boron arsenide can also be a promising material for photovoltaic and light detection applications. Direct measurement of photocarrier transport in cubic boron arsenide, however, has been challenging due to the small size of available high-quality samples.



Japan to invest $500 million in new company Rapidus to manufacture advanced chips

Japan said on Friday it will invest an initial 70 billion yen ($500 million) in a new semiconductor venture led by tech firms including Sony Group Corp and NEC Corp as it rushes to re-assert itself as a leading maker of advanced chips.

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The research team's study combines two feats: The crystal growth skills of the University of Houston team, and the imaging prowess at UC Santa Barbara. Combining the abilities of the scanning electron microscope and femtosecond ultrafast lasers, the UCSB team built what is essentially an extremely fast, exceptionally high-resolution camera.

"Electron microscopes have very good spatial resolution — they can resolve single atoms with their sub-nanometer spatial resolution — but they're typically very slow," Liao said, noting this makes them excellent for capturing static images.

"With our technique, we couple this very high spatial resolution with an ultrafast laser, which acts as a very fast shutter, for extremely high time resolution," Liao continued. "We're talking about one picosecond — a millionth of a millionth of a second. So we can make movies of these microscopic energy and charge transport processes." Originally invented at Caltech, the method was further developed and improved at UCSB from scratch and now is the only operational SUEM setup at an American university.

"What happens is that we have one pulse of this laser that excites the sample," explained graduate student researcher Usama Choudhry, the lead author of the Matter paper. "You can think of it like ringing a bell; it's a loud noise that slowly diminishes over time." As they "ring the bell," he explained, a second laser pulse is focused onto a photocathode ("electron gun") to generate a short electron pulse to image the sample. They then scan the electron pulse over time to gain a full picture of the ring. "Just by taking a lot of these scans, you can get a movie of how the electrons and holes get excited and eventually go back to normal," he said.

Among the things they observed while exciting their sample and watching the electrons return to their original state is how long the "hot" electrons persist.

"We found, surprisingly, the 'hot' electrons excited by light in this material can persist for much longer times than in conventional semiconductors," Liao said. These "hot" carriers were seen to persist for more that 200 picoseconds, a property that is related to the same feature that is responsible for the material's high thermal conductivity. This ability to host "hot" electrons for significantly longer amounts of time has important implications.

"For example, when you excite the electrons in a typical solar cell with light, not every electron has the same amount of energy," Choudhry explained. "The high-energy electrons have a very short lifetime, and the low-energy electrons have a very long lifetime." When it comes to harvesting the energy from a typical solar cell, he continued, only the low-energy electrons are efficiently being collected; the high-energy ones tend to lose their energy rapidly as heat. Because of the persistence of the high-energy carriers, if this material was used as a solar cell, more energy could efficiently be harvested from it.

With boron arsenide beating silicon in three relevant areas — charge mobility, thermal conductivity and hot photocarrier transport time — it has the potential to become the electronics world's next state-of-the-art material. However, it still faces significant hurdles — fabrication of high-quality crystals in large quantities — before it can compete with silicon, enormous amounts of which can be manufactured relatively cheaply and with high quality. But Liao doesn't see too much of a problem.

"Silicon is now routinely available because of years of investment; people started developing silicon around the 1930s and '40s," he said. "I think once people recognize the potential of this material, there will be more effort put into finding ways to grow and use it. UCSB is actually uniquely positioned for this challenge with strong expertise in semiconductor development."

Reference

Persistent hot carrier diffusion in boron arsenide single crystals imaged by ultrafast electron microscopy

Usama Choudhry, Fengjiao Pan, Xing He, Basamat Shaheen, Taeyong Kim, Ryan Gnabasik, Geethal Amila Gamage, Haoran Sun, Alex Ackerman, Ding-Shyue Yang, Zhifeng Ren, Bolin Liao

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Meta Materials Inc., a developer of high-performance functional materials and nanocomposites, today officially opened its new global headquarters and Centre of Excellence in Dartmouth, Nova Scotia. This 68,000 square foot state-of-the-art facility will house some of the world's leading scientists in metamaterials, advanced manufacturing, and nano-photonics.

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European Chips Act

The recent global chips shortage has disrupted supply chains, caused product shortages ranging from cars to medical devices, and in some cases even forced factories to close.

The European Chips Act, adopted by the Commission on 8 February 2022, seeks to strengthen the semiconductor ecosystem. It is composed of a Communication, which spells out the European Strategy and rationale behind the Chips Act, a proposal for a Regulation, and a Recommendation to Member States.

What is the European Chips Act?

The European Union has unveiled its new European Chips Act, a €43bn investment plan which aims to restore the continent's place as a leading hub of semiconductor innovation and build its chip manufacturing capabilities in the face of the ongoing global chip shortage. The plan is the latest part of the EU's bid for digital sovereignty, but experts have questioned whether it will have sufficient funding behind it to help Europe compete with the US and Asia, and if this investment will be directed in the right areas.

It will do so by focusing on 5 strategic objectives:

1- strengthening research and technological leadership;
2- building and reinforcing Europe's capacity to innovate in the design, manufacturing and packaging of advanced chips;
3- putting in place an adequate framework to increase production by 2030;
4- addressing the skills shortage and attracting new talent;
5- developing an in-depth understanding of global semiconductor supply chains.

The European Chips Act has 3 main components:

1- a Chips for Europe Initiative to support large-scale technological capacity building and innovation in cutting-edge chips;
2- a new framework to attract large-scale investments in production capacities and ensure the security of supply;
3- a coordination mechanism between the Member States and the Commission to monitor market developments and anticipate crises.

Read more on the European Commission website

CHIPS and Science Act of 2022

What Is the CHIPS and Science Act of 2022?

The CHIPS and Science Act of 2022—aka the Creating Helpful Incentives to Produce Semiconductors for America Act—refers to legislation signed into law by President Biden on Aug. 9, 2022, and adopted as Public Law No. 117-167.

Originally pegged at $52 billion, the passed legislation invests nearly $250 billion in a combination of semiconductor and other scientific research and development (R&D).

An additional $20 million appropriation goes to provide enhanced security for members of the U.S. Supreme Court and their families.

Key takeaways

1- The CHIPS and Science Act of 2022 invests nearly $250 billion in semiconductor and scientific research and development (R&D).
2- The act, which became law on Aug. 9, 2022, mainly seeks to implement previously authorized programs under the CHIPS for American Act 2021 and authorize the largest publicly funded R&D program in the country's history.
3- The legislation seeks to return the United States to dominance in chipmaking and to combat supply chain issues that have arisen from the country's decline in science and technology.
4- Included in the legislation is a $20 million appropriation to provide security for members of the U.S. Supreme Court and their families.
5- Once fully implemented, the CHIPS and Science Act of 2022 will represent the largest publicly funded five-year investment in research and development in the country's history.

The CHIPS and Science Act of 2022 has two main objectives: implementing previously authorized programs under the CHIPS for America Act of 2021, and authorizing the most extensive publicly funded five-year R&D program in the country's history.

In January 2021, Congress passed the CHIPS for America Act into law. This legislation authorized the Department of Commerce (DOC), Department of Defense (DoD), and Department of State (DOS) to develop onshore domestic manufacturing of semiconductors. This legislation stemmed from the fact that only 12% of chips are currently manufactured in the U.S., compared with 37% in the 1990s.

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